

FN1241
Audio D/A Converter
Specification Data Sheet

Ver.001218

Niigata Seimitsu Co., Ltd.

FN1241

Product Overview:

FN1241 is digital audio 2CH-1 bit D/A converter IC that has fluency type data compensation filter built-in.

DAC part adopted newly developed high stability wide range swing suppression method. It reproduces wide range output signals generated by the compensation filter. Analog output is four-value differential PWM output. Addition of external differential circuit brings high quality audio signals.

Features:

By using 8 times oversampling Fluency digital filter, 16 bit input is converted to 24 bit by interpolation.

High performance 1 bit DAC

- 16 times oversampling interpolation filter
- Bandwidth: 40 kHz

Note : The above figures are given when master clock SCLK = 512 fs
and sampling frequency = 44.1 kHz.

Sampling Frequency: supports sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz

Audio data format: MSB first right-justified, MSB first left-justified, IIS
(available for 16, 20, and 24 bit interface)

Master clock frequency: 512 fs, 384 fs.

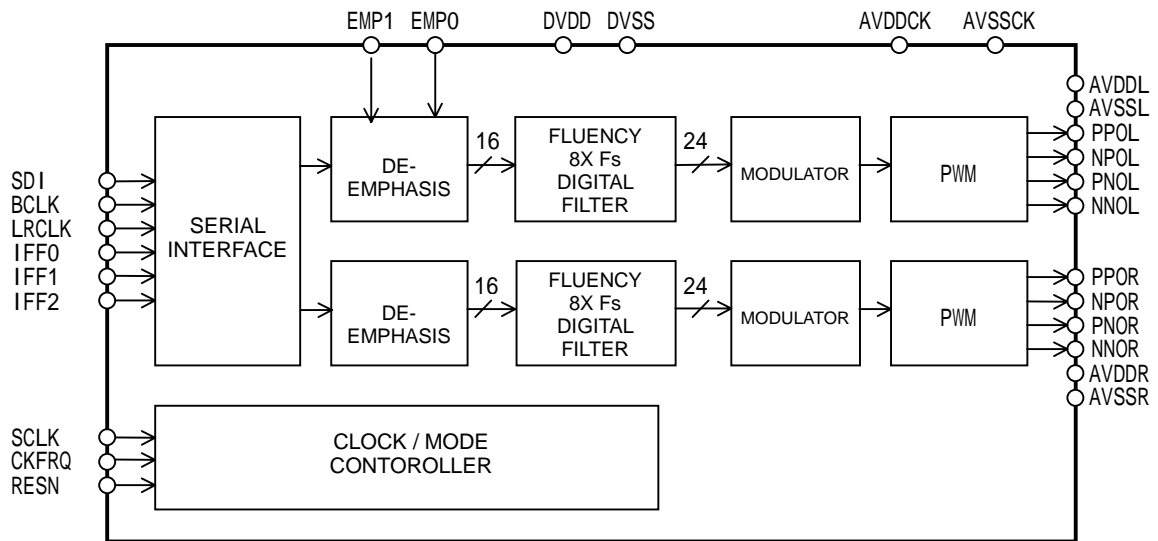
Digital de-emphasis filter for sampling frequencies of 32 kHz, 44.1 kHz and 48 kHz.

Single 3.3 V power supply: available for 3.3 V CMOS interface and 5 V TTL interface

Applications:

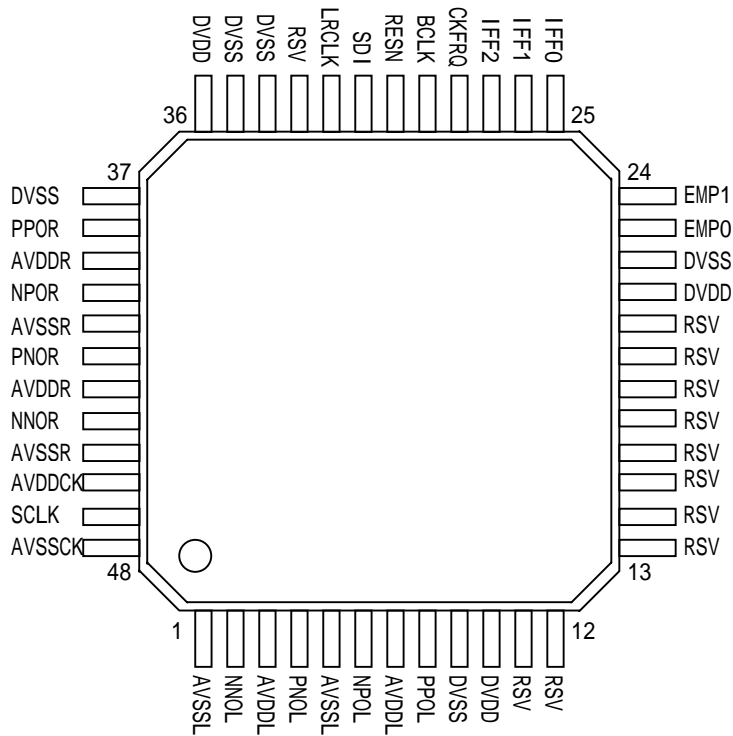
The FN1241 is suitable for use in middle-class or high-class digital audio equipment, which demands good sound quality, such as CD players for use in a car or at home, digital TV, and set top box.

Block diagram:



Package:

48 pin QFP (0.8mm pitch)



Pin Function Descriptions:

| Pin | Pin Name | I/O | Description | |
|-----|----------|-----|---|--|
| 1 | AVSSL | - | Left Channel Analog Ground | |
| 2 | NNOL | O | Left Channel Analog Audio Output (- / -) | |
| 3 | AVDDL | - | Left Channel Analog Power Supply (3.3V) | |
| 4 | PNOL | O | Left Channel Analog Audio Output (- / +) | |
| 5 | AVSSL | - | Left Channel Analog Ground | |
| 6 | NPOL | O | Left Channel Analog Audio Output (+ / -) | |
| 7 | AVDDL | - | Left Channel Analog Power Supply (3.3V) | |
| 8 | PPOL | O | Left Channel Analog Audio Output (+ / +) | |
| 9 | DVSS | - | Digital Ground | |
| 10 | DVDD | - | Digital Power Supply (3.3V) | |
| 11 | TEST | I | Test Pin. Connect to DVSS. | |
| 12 | TEST | I | Test Pin. Connect to DVSS. | |
| 13 | TEST | I | Test Pin. Connect to DVSS. | |
| 14 | TEST | I | Test Pin. Connect to DVSS. | |
| 15 | TEST | I | Test Pin. Connect to DVSS. | |
| 16 | RSV | - | Leave this pin open. | |
| 17 | RSV | - | Leave this pin open. | |
| 18 | RSV | - | Leave this pin open. | |
| 19 | RSV | - | Leave this pin open. | |
| 20 | RSV | - | Leave this pin open. | |
| 21 | DVDD | - | Digital Power Supply (3.3V) | |
| 22 | DVSS | - | Digital Ground | |
| 23 | EMP0 | I | De-emphasis Filter Select. (EMP1, EMP0) = 00 : OFF (no de-emphasis) = 01 : 48KHz = 10 : 44.1KHz = 11 : 32KHz | |
| 24 | EMP1 | I | | |
| 25 | IFF0 | I | | Input Data Format Select. (IFF2, IFF1, IFF0) = 000 : 16bitMSB first right-justified = 001 : 20bitMSB first right-justified = 010 : 24bitMSB first right-justified = 100 : 16,20,24bitLSS format = 101 : - = 110 : 16,20,24bitMSB first left-justified |
| 26 | IFF1 | I | | |
| 27 | IFF2 | I | | |
| 28 | CKFRQ | I | Master Clock Frequency Select: 384fs at LOW and 512fs at HIGH | |
| 29 | BCLK | I | Serial Data Clock Input. 64FS or 32FS when SCLK = 512FS 64FS, 48FS or 32FS when SCLK = 384FS | |
| 30 | RESN | I | Reset input. Low active. | |
| 31 | SDI | I | Serial Audio Data Input | |
| 32 | LRCLK | I | Left/Right Clock Input | |
| 33 | RSV | - | Leave this pin open. | |
| 34 | DVSS | - | Digital Ground | |
| 35 | DVSS | - | Digital Ground | |
| 36 | DVDD | - | Digital Power Supply (3.3V) | |
| 37 | DVSS | - | Digital Ground | |
| 38 | PPOR | O | Right Channel Analog Audio Output (+ / +) | |
| 39 | AVDDR | - | Right Channel Analog Power Supply (3.3V) | |
| 40 | NPOR | O | Right Channel Analog Audio Output (+ / -) | |
| 41 | AVSSR | - | Right Channel Analog Ground | |
| 42 | PNOR | O | Right Channel Analog Audio Output (- / +) | |

| | | | |
|----|--------|---|--|
| 43 | AVDDR | - | Right Channel Analog Power Supply (3.3V) |
| 44 | NNOR | O | Right Channel Analog Audio Output (- / -) |
| 45 | AVSSR | - | Right Channel Analog Ground |
| 46 | AVDDCK | - | Power Supply (3.3V) |
| 47 | SCLK | I | System Clock Input. This pin inputs 384fs when CLKFRQ=LOW, and 512fs when CLKFRQ=HIGH. |
| 48 | AVSSCK | - | System Clock Ground |

Electrical Characteristics:

- Absolute maximum ratings* (Ta = 25 , Vss = 0 V)

| Parameter | Symbol | Rating | Unit |
|---------------------|--------|-----------------|------|
| Supply voltage | VDD | -0.3 ~ +4.6 | V |
| Input voltage | VI | -0.3 ~ VDD+ 0.3 | V |
| Output voltage | VO | -0.3 ~ VDD+ 0.3 | V |
| Storage temperature | Tstg | -55 ~ +150 | |

Note*: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation under any of these conditions is not guaranteed.

- Recommended operating conditions

| Parameter | | Symbol | MIN | TYP | MAX | Unit |
|--------------------------------|---------------|--------------------|-----|-----|-----|------|
| Operating Temperature (Note**) | 3.3V CMOS I/F | Ta | -30 | +25 | +85 | |
| | 5V TTL I/F | Ta | 0 | +25 | +70 | |
| Supply Voltage | | DVDD, AVDDL, AVDDR | 3.0 | 3.3 | 3.6 | V |

Note**: For operating temperature, please contact our marketing department.

• Analog Performance

Test Conditions unless otherwise noted:

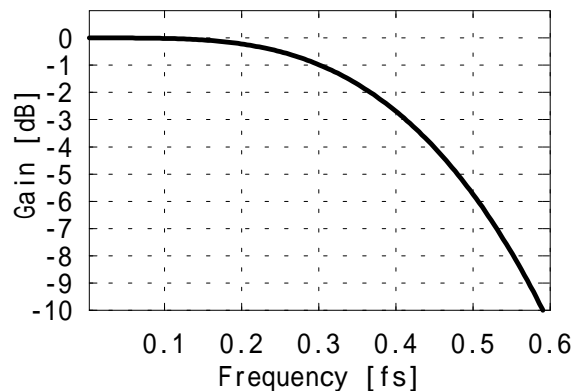
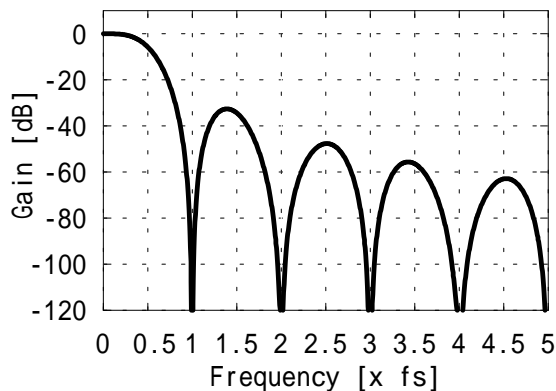
Ta = 25 / AVDD, DVDD = 3.3 V / fs = 44.1 kHz / SCLK = 512 fs / Input Signal = 1 kHz
16 bit data / Measurement Bandwidth = 20 Hz to 20 kHz

| | | Condition | MIN | TYP | MAX | UNIT |
|---|-------------------------|--|-----------------------------|----------|-----|------|
| 1 | Resolution | | 16 | | | Bit |
| 2 | Dynamic Characteristics | THD+N | Vo = 0dB | 0.002 | | dB |
| | | Dynamic Range | Vo = -60dB, EIAJ A-weighted | 106 | | dB |
| | | S/N Ratio | EIAJ A-weighted | 106 | | dB |
| | | Channel Separation | 1 kHz | 106 | | dB |
| 3 | DC Characteristics | On-state resistance of PWM output buffer | 3 | 5 | 7.5 | |
| 4 | Analog Output | Output Voltage | - | 0.49*VDD | - | Vpp |
| | | Center Voltage | - | VDD/2 | - | V |
| | | Load Resistance | 100 | - | - | K |
| 5 | Power Supply Current | DVDD | DVDD=3.3V | 19 | | mA |
| | | AVDDL, AVDDR | AVDDL=AVDDR=3.3V | 1.5 | | mA |
| | | AVDDCK | AVDDCK=3.3V | 0.5 | | mA |

Note: Specifications subject to change without notice.

• Digital Filter Characteristics

| | | Condition | MIN | TYP | MAX | UNITs |
|---|-----------------|------------------|-----|------|-----|-------|
| 1 | Passband | -3 dB fs=44.1KHz | - | 18.4 | - | KHz |
| | | -6 dB fs=44.1KHz | - | 22.5 | - | KHz |
| 2 | Passband Ripple | | - | 0 | - | dB |



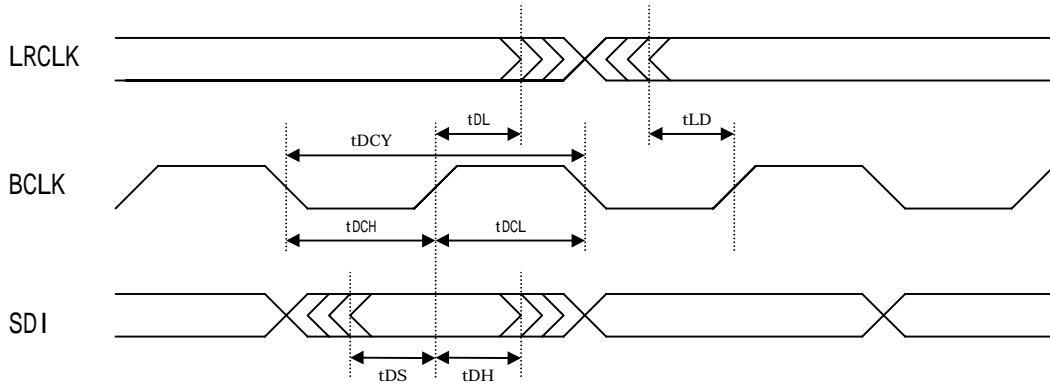
• De-emphasis Filter Characteristics

| | Condition | MIN | TYP | MAX | Unit |
|-------------------|--------------|-----|------|-------------|------|
| De-emphasis Error | fs = 44.1kHz | - | - | -0.2 ~ +0.2 | dB |
| Group Delay | | - | 2/fs | - | sec |

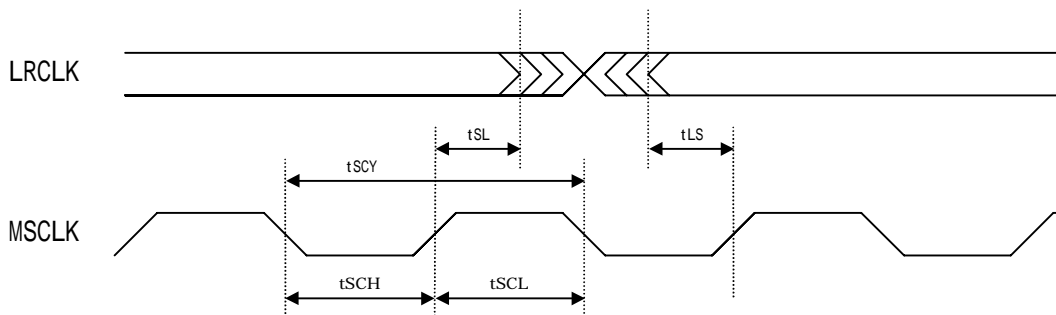
• DC Characteristics

| Parameter | Symbol | MIN | TYP | MAX | Unit |
|---------------------|-----------------|-----------------------|-----|-----------------------|------|
| Input Voltage High | V _{IH} | 0.7 × V _{DD} | --- | V _{DD} | V |
| Input Voltage Low | V _{IL} | 0 | --- | 0.3 × V _{DD} | V |
| Output Voltage High | V _{OH} | V _{DD} - 0.6 | --- | --- | V |
| Output Voltage Low | V _{OL} | --- | --- | 0.4 | V |

• AC Characteristics

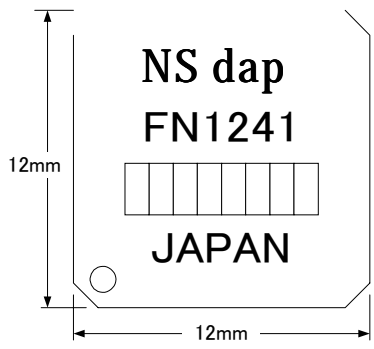
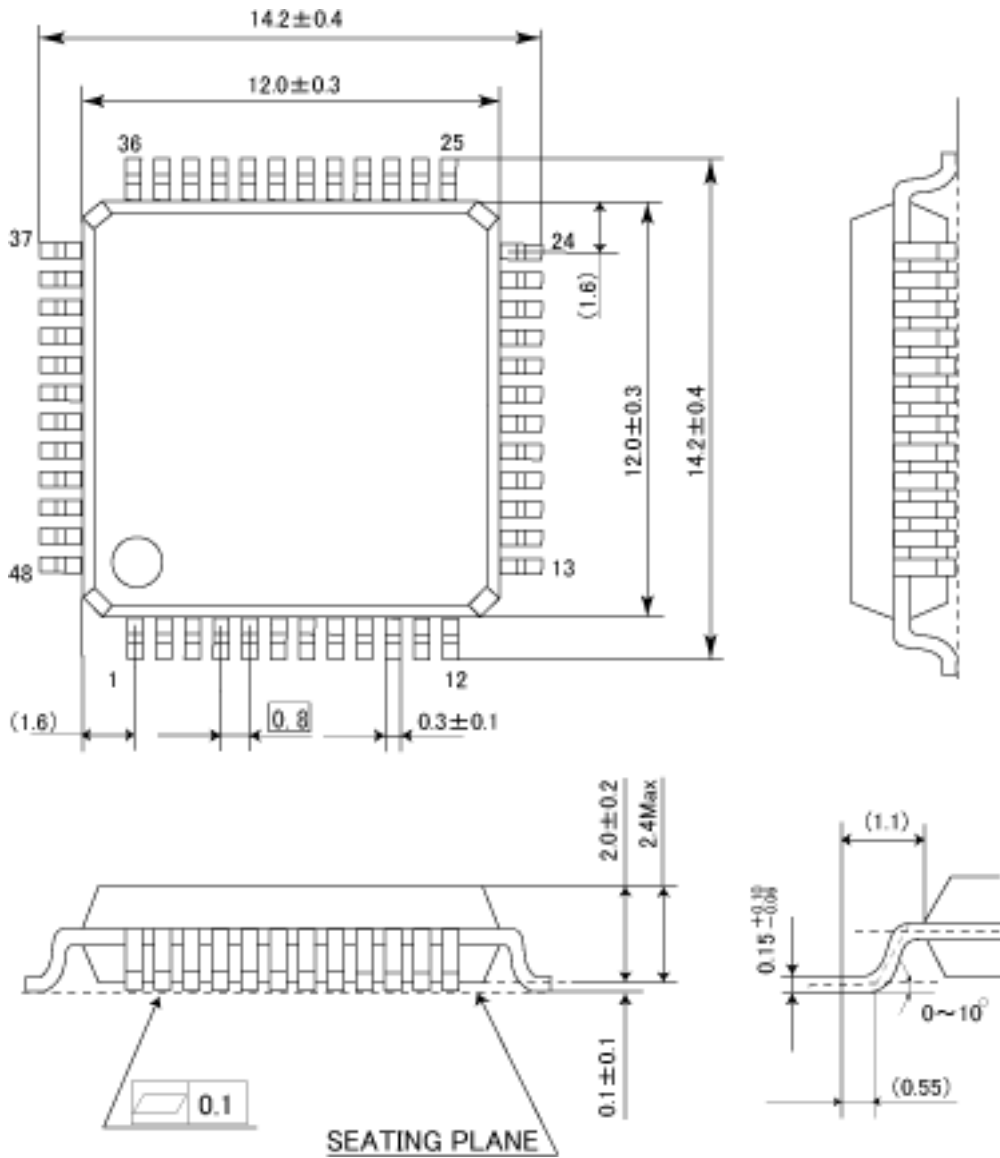


| Parameter | Symbol | MIN | TYP | MAX | Unit |
|--------------------------------|------------------|-----|-----|-----|------|
| BCLK Period | t _{DCY} | 300 | - | - | ns |
| BCLK HI Pulsewidth | t _{DCH} | 150 | - | - | ns |
| BCLK LO Pulsewidth | t _{DCL} | 150 | - | - | ns |
| BCLK Rising Edge -> LRCLK Edge | t _{DL} | 50 | - | - | ns |
| LRCLK Edge -> BCLK Rising Edge | t _{LD} | 50 | - | - | ns |
| SDI Setup Time | t _{SDS} | 50 | - | - | ns |
| SDI Hold Time | t _{SDH} | 50 | - | - | ns |



| Parameter | Symbol | MIN | TYP | MAX | Unit |
|----------------------------------|------------------|-----|-----|-----|------|
| SCLK Period | t _{SCY} | 40 | - | - | ns |
| SCLK HI Pulsewidth | t _{SCH} | 20 | - | - | ns |
| SCLK LO Pulsewidth | t _{SCL} | 20 | - | - | ns |
| MSCLK Falling Edge -> LRCLK Edge | t _{SL} | 10 | - | - | ns |
| LRCLK Edge -> MSCLK Rising Edge | t _{LS} | 10 | - | - | ns |

Package Marking



50 pieces FN1241 are packed in a damp-proof hard-case.