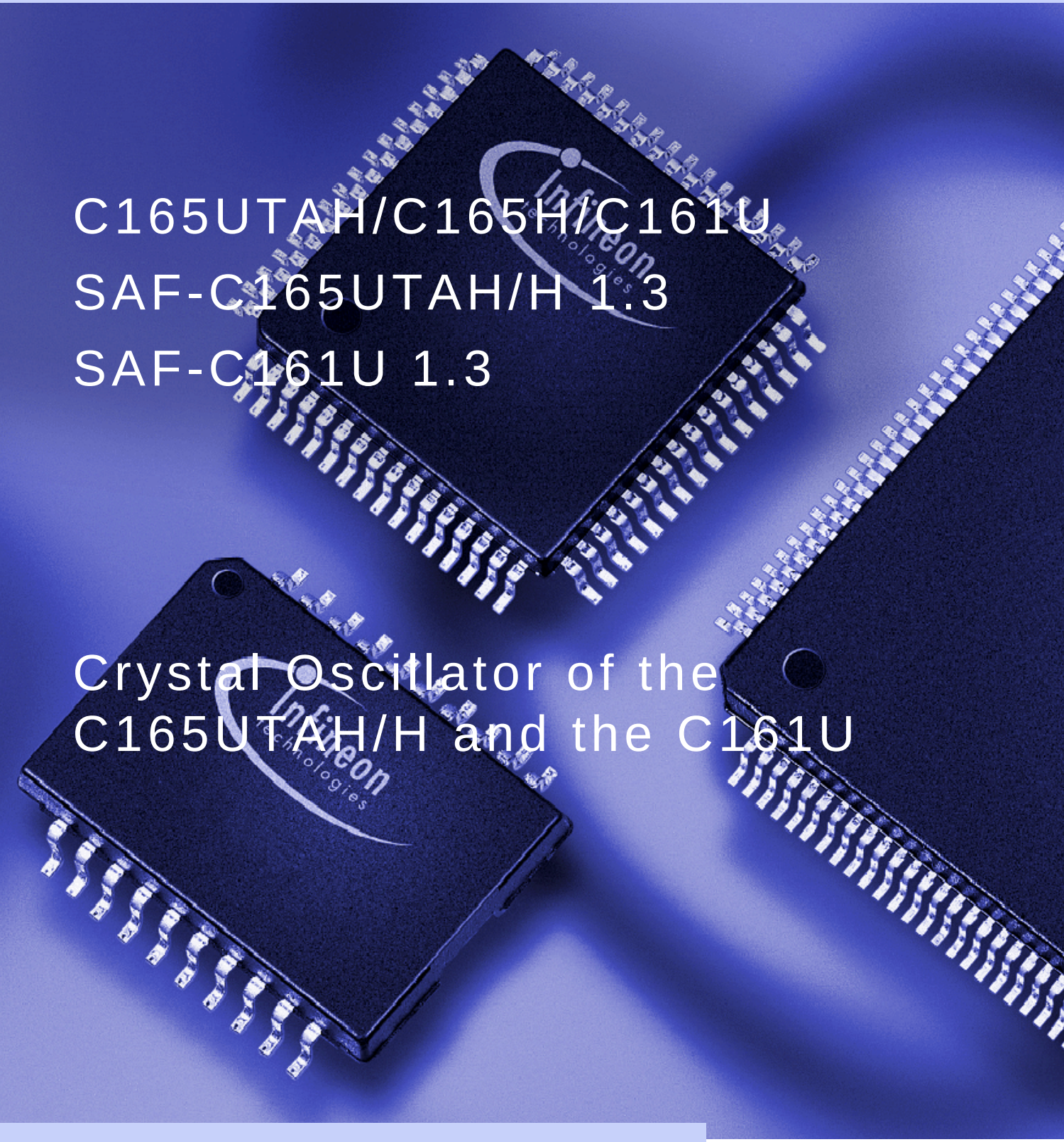
Application Note, DS1, Oct. 2000

C165UTAH/C165H/C161U
SAF-C165UTAH/H 1.3
SAF-C161U 1.3



Crystal Oscillator of the C165UTAH/H and the C161U

Wired Communication

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1 Introduction

This application note provides recommendations concerning the selection of the right composition of external components connected to the main oscillator in the C165UTAH/ C165H/C161U. The IC oscillator and the quartz crystal do not always work together properly with some external circuits. This document describes the measurements required in order to select appropriate external circuits. Its general guidelines can be applied to all Pierce oscillators that use an oscillator-inverter. Furthermore, guidelines are provided for the selection of suitable quartz crystals, depending on the application.

2 Oscillator-Inverter

The C165UTAH/H / C161U chip includes the active part of the oscillator (also called oscillator-inverter). The on-chip oscillator-inverter can either run with an external crystal and appropriate external oscillator circuitry (also called oscillator circuitry or passive part of the oscillator), or it can be driven by an external oscillator. The external oscillator directly connected to XTAL1 (leaving XTAL2 open) feeds the external clock signal to the internal clock circuitry.

The oscillator input XTAL1 and output XTAL2 connect the internal CMOS Pierce oscillator to the external crystal. The oscillator provides an inverter and a feedback element. The resistance of the feedback element is in the range of 0.5 to 1 MΩ.

3 Fundamental Mode and 3rd Overtone

Depending on the system demands, there are two different kinds of oscillator modes available. The external quartz crystal can be prepared for the fundamental mode or for the 3rd overtone mode.

The standard external oscillator circuitry for fundamental mode (**Figure 1**) includes the crystal, two low-end capacitors, and a series resistor R_{X2} to limit the current through the crystal. A test resistor R_Q may be inserted temporarily to measure the oscillation allowance of the oscillator circuitry. How to check the start-up reliability will be explained in detail in **Chapter 6**.

For the 3rd overtone mode, an additional inductance/capacitance combination (L_X/C_{X2}) is required to suppress oscillation in the fundamental mode and bias voltage (C_X) at the XTAL2 output. Fundamental mode is suppressed via phase shift and filter characteristics of the L_X/C_{X2} network. The formula f_{LXCX2} in **Chapter 5.3** calculates the frequency at which the inductive behavior of the L_X/C_{X2} network changes to capacitive. The oscillation condition in 3rd overtone mode needs a capacitive behavior for f_{3rd} and an inductive one for f_{fund}.

The 3rd overtone mode is often used in applications where the crystal is exposed to strong mechanical vibrations, because 3rd overtone crystals have a higher mechanical stability than fundamental mode crystals with the same frequency.

There are various ways to connect the L_X/C_X network for 3rd overtone to the oscillator circuit. The L_X/C_X network theoretically can be connected to C_{X1} or C_{X2}. This application note recommends the connection to C_{X2} (**Figure 1**) because a little variation of L_X, caused by production deviation has more affect on the oscillator start-up behavior at the XTAL1 input than at the XTAL2 output. Furthermore, the additional hardware for 3rd overtone mode receives additional electrical noise from the system. In a $C_{X1}/L_X/C_X$ combination, the noise will be amplified via the oscillator inverter. In a $C_{X2}/L_X/C_X$ combination, the noise will be damped by the quartz crystal. Depending on the quality of the printed circuit board design, a $C_{X1}/L_X/C_X$ combination can have a negative effect on the start-up behavior of the oscillator.

Note: There is no need to change existing working designs that use the $C_{X1}/L_X/C_X$ combination when the Safety Factor SF is within the desired range.

Note: The resistor R_{X2} should only be used, if the maximum specified drive level of the quartz crystal is exceeded.

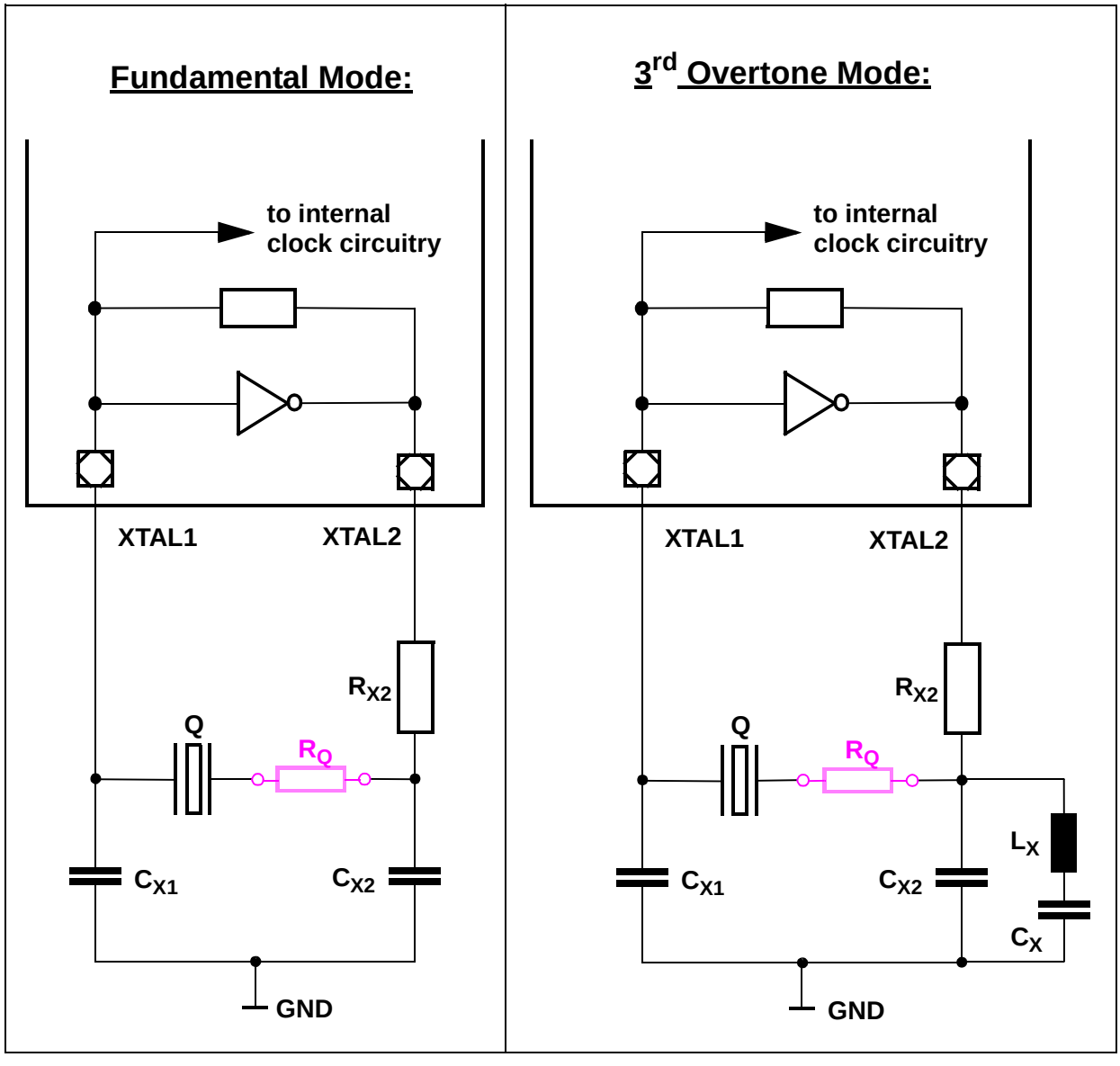

Figure 1 Oscillator Modes

4 Oscillator Start-up Time

The main oscillator starts oscillating after the internal reset sequence is finished. Based on small electrical system noise or thermic noise caused by resistors, the oscillation starts with a very small amplitude. Due to the amplification of the oscillator-inverter, the oscillation amplitude increases and reaches its maximum after a certain time period t_{st_up} (start-up time). The oscillator start-up time depends on the oscillator frequency. Typical values of the start-up time are in the range of 0.1 ms ≤ t_{st_up} ≤ 4 ms for the maximum specified frequency of 20 MHz. Theoretically, the oscillator-inverter performs a phase shift of 180°, and the external circuitry performs a phase shift of 180° to fulfill the oscillation condition of an oscillator. A total phase shift of 360° is necessary.

In reality, the real phase shift of the oscillator-inverter depends on the oscillator frequency, and is approximately 100° to 210°. It is necessary to compose the external components in a way that a total phase shift of 360° is performed. This can be achieved by a variation of C_{x1} and C_{x2}.

The definition of the oscillator start-up time is not a well-defined value in literature. Generally it depends on the power-supply rise time dV_{DD}/dt after wakeup, the electrical system noise, and on the oscillation amplitude. For this application, the oscillator start-up time t_{st_up} is defined from $V_{DD}/2$ to $0.9*V_{OSC\_max}$ of the stable oscillation (**Figure 2**).

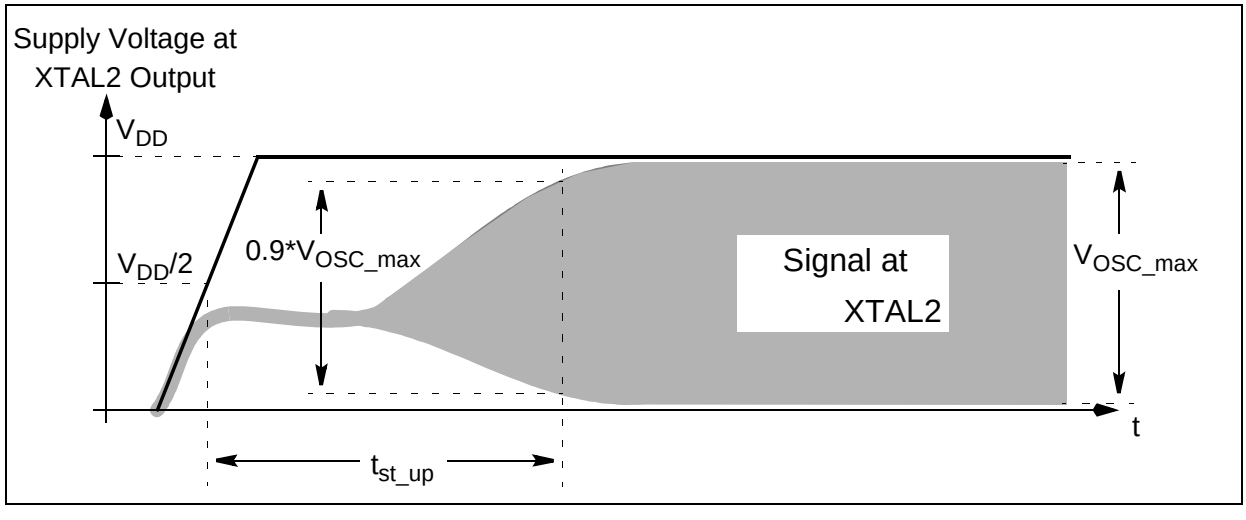

Figure 2 Oscillator Start-up Time

5 Drive Level

5.1 Measurement of Drive Current

The amplitude of mechanical vibration of the quartz crystal increases proportionally to the amplitude of the applied current. The power dissipated in the load resonance resistance R_L (in other technical descriptions also called “effective resistance” or “transformed series resistance”) is given by the drive level P_W. The peak-to-peak drive current I_{pp} is measured in the original application with a current probe directly at the crystal lead (**Figure 3**). The drive level is calculated with the formulas shown in **Chapter 5.2** and **Chapter 5.3**. The drive level is mainly controlled via R_{X2} and C_{X1}, but C_{X2} also has an influence.

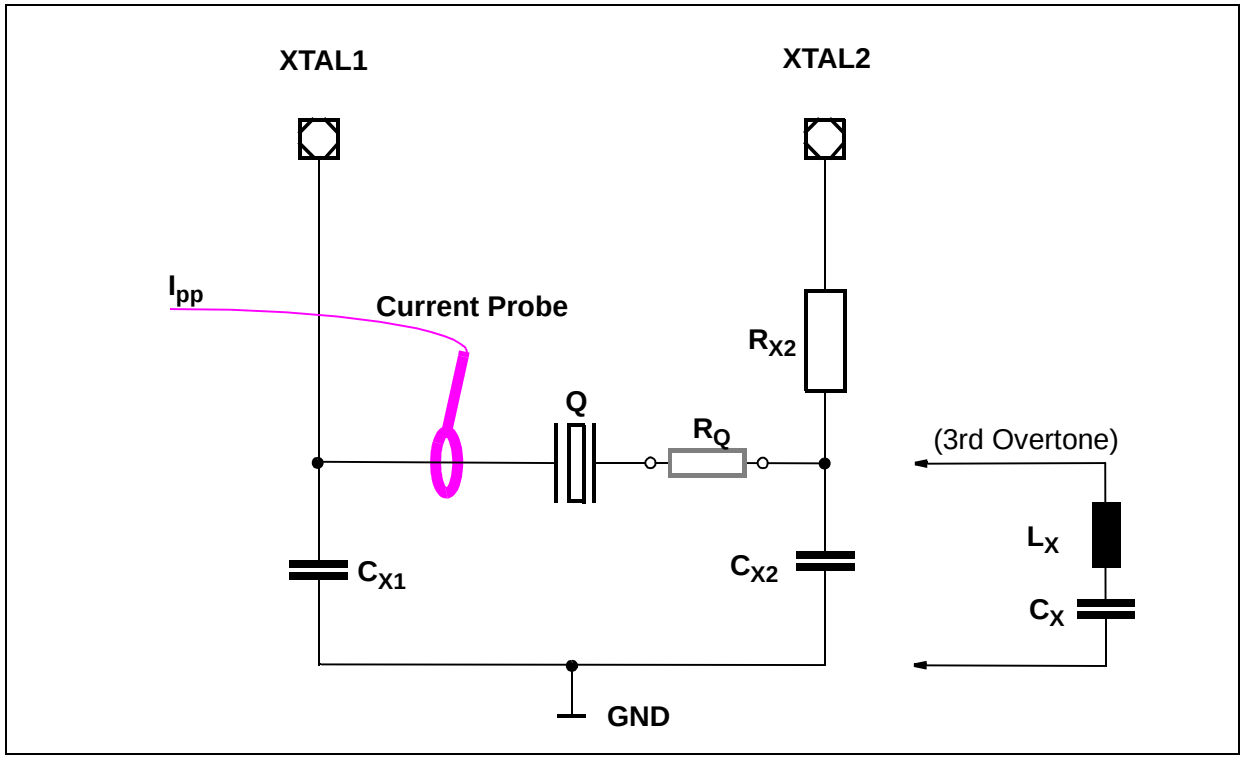

Figure 3 Measurement of Drive Current with a Current Probe

5.2 Drive Level Calculation for Fundamental Mode

The maximum and minimum drive level allowed depend on the crystal used, and should be within the typical range of 50 µW ≤ P_W ≤ 800 µW. For detailed information, see the quartz crystal data sheet.

The load resonance resistance R_{Ltyp} is calculated with the typical values of the quartz crystal and of the system. The formula is shown below. The typical values of R_1 (R_{1typ}) and C_0 (C_{0typ}) are supplied by the crystal manufacturer. The stray capacitance C_S consists of the capacitance of the board layout, the input capacitance of the on-chip oscillator-inverter, and other parasitic effects in the oscillator circuit. A typical value of the input pin capacitance of the inverter is 3 pF. A typical value of the stray capacitance in a normal system is C_S = 5 pF.

Drive level: $$P_W = I_Q^2 \cdot R_{Ltyp}$$

Drive current: $$I_Q = \frac{Ipp}{2 \cdot \sqrt{2}}$$ (for sine wave)

Load resonance resistance: $$R_{Ltyp} = R_{1typ} \cdot \left[1 + \frac{C_{0typ}}{C_L}\right]^2$$

Load capacitance: $$C_L = \frac{C_{X1} \cdot C_{X2}}{(C_{X1} + C_{X2})} + C_S$$

5.3 Drive Level Calculation for 3rd Overtone Mode

The calculation of the drive level in 3rd overtone mode is equal to the calculation for fundamental mode apart from the calculation of the load capacitance. The formulas below show the relationships between load capacitance, circuit components and frequencies in 3rd overtone.

Load capacitance: $$C_L = \frac{C_{X1} \cdot C_{X2rest}}{C_{X1} + C_{X2rest}} + C_S$$

C_{X2} rest capacitance: $$C_{X2rest} = C_{X2} - \frac{1}{(2\pi f_{3rd})^2 \cdot L_X}$$

Resonance frequency of C_{X2} and L_X (Thomson formula):

$$f_{LXCX2} = \frac{1}{2\pi \cdot \sqrt{L_X \cdot C_{X2}}}$$

Relation between f_{fund} and f_{3rd}: $$f_{LXCX2} \approx \left(\frac{f_{fund} + f_{3rd}}{2} = 2 \cdot f_{fund} \right)$$

6 Start-up- and Oscillation Reliability

Most problems with the C165UTAH/H / C161U oscillator occur during the oscillation start-up time. During start-up time, the drive level of the oscillation begins at the minimum value and increases to the maximum. During that time, the resistance of the crystal can reach high values because crystals show resistance dips depending on the drive level and the temperature. This effect is called Drive Level Dependence (DLD). The DLD of a quartz crystal depends on its quality, and can alter during production and during the life time of the crystal. If the resistance dips of the crystal increase in a range where the amplification of the oscillator is lower than one, the oscillation cannot start.
Therefore it is strongly recommended to check the start-up and oscillation reliability.
This test is done with the negative resistance method.

For further details, please refer to the following IEC standards:
IEC 122-2-1: Quartz crystal units for microprocessor clock supply
IEC 444-6: Measurement of Drive Level Dependence (DLD)

6.1 Negative Resistance Method

The oscillator can be divided into the on-chip oscillator-inverter and the external circuitry. The oscillator circuitry can be simplified as shown in **Figure 4**. The load capacitance C_L includes C_{X1}, C_{X2} and the stray capacitance C_S. The amplification ability of the oscillator-inverter is replaced with a negative resistance $-R_{INV}$, and the quartz crystal is replaced by the load resonance resistance R_L (effective resistance) and the effective reactance L_Q.

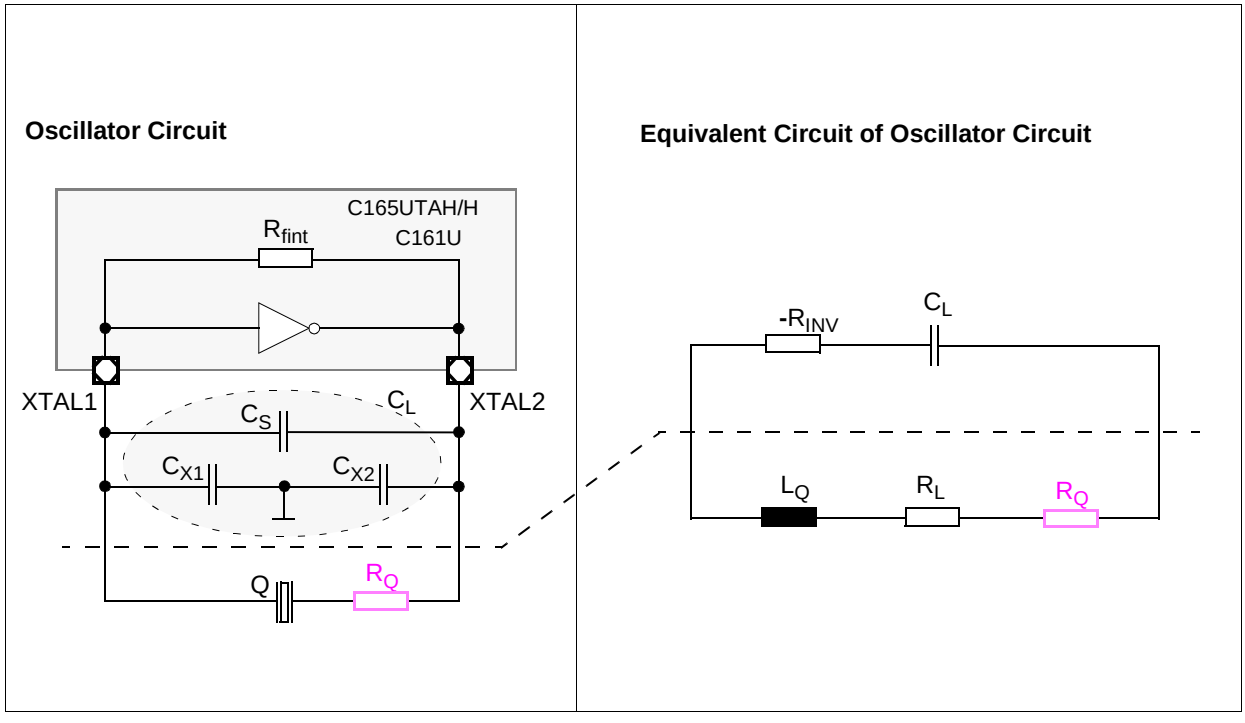

Figure 4 Equivalent Circuit for Negative Resistance Method

The condition required for oscillation is:

$$|-R_{INV}| \geq R_L$$

The negative resistance has to be large enough to cover all possible variations of the oscillator circuitry, in order to guarantee problem-free operation. The negative resistance can be analyzed by connecting a series test resistor R_Q to the quartz crystal (**Figure 4**) in order to find the maximum value R_{Qmax} that keeps the circuit oscillating. R_L is the resistance of the quartz crystal at oscillating frequency and creates the power dissipation.

Negative resistance: $$|-R_{INV}| = R_L + R_{Qmax}$$

6.2 Measurement of Start-up- and Oscillation Reliability

As described above, the resistance of a crystal depends on the drive level. A simple method to check the start-up and oscillation reliability of the oscillator is to insert a test resistor R_Q in series with the quartz crystal (**Figure 3**).
The value of R_Q is increased until the oscillation does not start any more. R_Q is then decreased until oscillation starts again. This final value of R_{Qmax} is used for further calculations of the Safety Factor SF.

Note: The series resistor R_Q should be an SMD device or a potentiometer that is suitable for RF (Radio Frequency). Depending on the RF behavior of the potentiometer, the results of using an SMD resistor or a potentiometer may differ. The result of the potentiometer is sometimes worse than the one of the SMD resistor. Therefore, you should use the potentiometer in order to find the final value R_{Qmax}, and then verify R_{Qmax} with a SMD resistor.

Note: The start-up and oscillation reliability can be influenced by using a socket for the C165UTAH/H / C161U *chip during measurement. The influence is caused by the additional inductance and capacitance of the socket. Start-up and oscillation reliability should be measured in a system resembling that expected to be used for mass production (i.e., with or without a socket).*

Note: Depending on the system demands, start-up and oscillation reliability should also be verified at various supply voltages and temperatures.

Table 1 Element Range for Test

Element	Range
$C_{X1} = C_{X2}$	0 - 39 pF
R_{X2}	0 - 1 kΩ
3rd Overtone: L_X	1 - 15 µH
3rd Overtone: C_X	1 - 10 nF

The measurement procedure described for R_{Qmax} has to be performed for different values of R_{X2}, C_{X1} and C_{X2}. During the test, the values of the different elements have to be changed one after another, and the results noted in a table. A typical protocol table is shown in **Table 2**. For the first test, it is recommended to use $C_{X1} = C_{X2}$. A suggestion for the range is given in **Table 1**. The range of the elements depends on the quartz crystal used, and on the characteristics of the printed circuit board. After the test, the measured values should be displayed graphically (**Figure 5**).

Start-up- and Oscillation Reliability

Measuring the start-up and oscillation reliability for the 3rd overtone mode is more work than for the fundamental mode. The relation between the values of L_X and C_{X2} is given via the formulas in **Chapter 5.3**. When C_X lies within the recommended range, theoretically it has no effect on the start-up behavior of the oscillator; however, in a system, the parasitic inductive part of C_X can have a little influence. C_X is needed only in order to suppress bias voltage at XTAL2 output. Recommended values are shown in **Table 1**.

Table 2 Example of a Protocol Table

R_{X2}= ... Ohm			
$C_{X1} = C_{X2}$	I_Q or P_w	R_{Qmax}	Comment
0 pF			
2.7 pF			
. . .			
10 pF			
. . . .			
39 pF			

6.3 Safety Factor

The Safety Factor SF is the relationship between maximum test resistance R_{Qmax}, which can be added in series to the quartz crystal while it is still oscillating, and the maximum load resonance resistance R_{Lmax}. It gives a feeling of how much the resistance of the passive part of the oscillator circuitry can be increased (caused by the drive level dependence of the crystal) until the oscillation is suppressed. Depending on production quality and long-term behavior of all parts of the oscillator circuitry, the SF needs a certain minimum value to grant a problem-free operation of the oscillator for mass production and during life time. **The qualification of the SF as shown in Table 3 is based on the experience of the Tele Quarz Group (see Chapter 9).**

Safety Factor: $$SF = \frac{R_{Qmax}}{R_{Lmax}}$$

Load resonance resistance: $$R_{Lmax} = R_{1max} \cdot \left[1 + \frac{C_{0typ}}{C_L}\right]^2$$

Table 3 Assessing the Safety Factor

Safety Factor	Assessment
SF < 1.5	unsuitable
1.5 ≤ SF < 2	risky
2 ≤ SF < 3	suitable
3 ≤ SF < 5	safe
SF ≥ 5	very safe

Note: It is strongly recommended that the user determines whether the SF is sufficient for the system. In case the SF is not sufficient in the fundamental mode, it is possible to use the 3rd overtone mode.

6.4 Determination of the Safety Factor with C165UTAH/H / C161U

To determine if the oscillation starts correctly at a certain test resistance R_Q, the following procedure is recommended:

1. Issue a hardware reset.
2. The processor starts automatically after the internal reset sequence has been finished
3. Determine if the CPU starts to fetch code from the external memory space by activating the ALE signal
4. The external memory activated by CS0 at address 0x0000 must contain a proper startup code. The bit CLKEN has to be set within this code, to enable the system clock output at P3.15. To be sure that the oscillation starts properly and therefore the firmware works properly, some accesses to the external memory and/or standard perpherals should be processed and verified.
5. After this, the correct frequency of the oscillation should be verified at XTAL2 and the system operating frequency can be monitored at P3.15.

Positive results should be obtained every time the sequence is repeated. Several runs are recommended.

6.5 Qualification of the Results

The bases for the evaluation of the measured results are the protocol tables. The results are displayed in evaluation diagrams as shown in **Figure 5**. One evaluation diagram should be used for each protocol table with a fixed R_{X2}. The evaluation diagram includes the characteristic curve for the SF and the drive level P_W. It is also possible to display the resistance of the test resistor R_Q and the crystal current I_Q. In the evaluation diagram, the specified minimum and maximum values of P_W (I_Q) of the crystal used can be marked. Results a fixed range can thus be determined for the allowed capacitance of C_{X1} and C_{X2}. Depending on the circuit composition, the characteristic curve of SF (R_{Qmax}) very often includes a maximum for capacitance values in the C_{X1}/ C_{X2} range of 0 pF to 3 pF. The recommended range for SF (R_{Qmax}) should be in the falling area of the characteristic curve, as marked in the diagram. Depending on the area selected for SF (R_{Qmax}), a specific range for C_{X1} and C_{X2} is given.

Two areas for C_{X1} and C_{X2} are given, one by P_W (I_Q) and the other by SF (R_{Qmax}). The capacitive values that are available in both areas are allowed for the oscillator circuit (see marked area in the diagram). This analysis has to be done for every R_{X2} value. The final selection of the components should take into account the necessary safety level, frequency, quality of the start-up behavior of the oscillator, start-up time of the oscillation, and the specified load capacitance C_L of the crystal.

Note: It is not recommended to include the maximum of SF (R_{Qmax}) because in many cases the gradient of the characteristic curve between 0 pF and 3 pF is very high. If C_{X1} and C_{X2} were chosen in that area, small parameter variations of the components used during production could significantly reduce the safety level. As consequence, the oscillator does not work in this case.

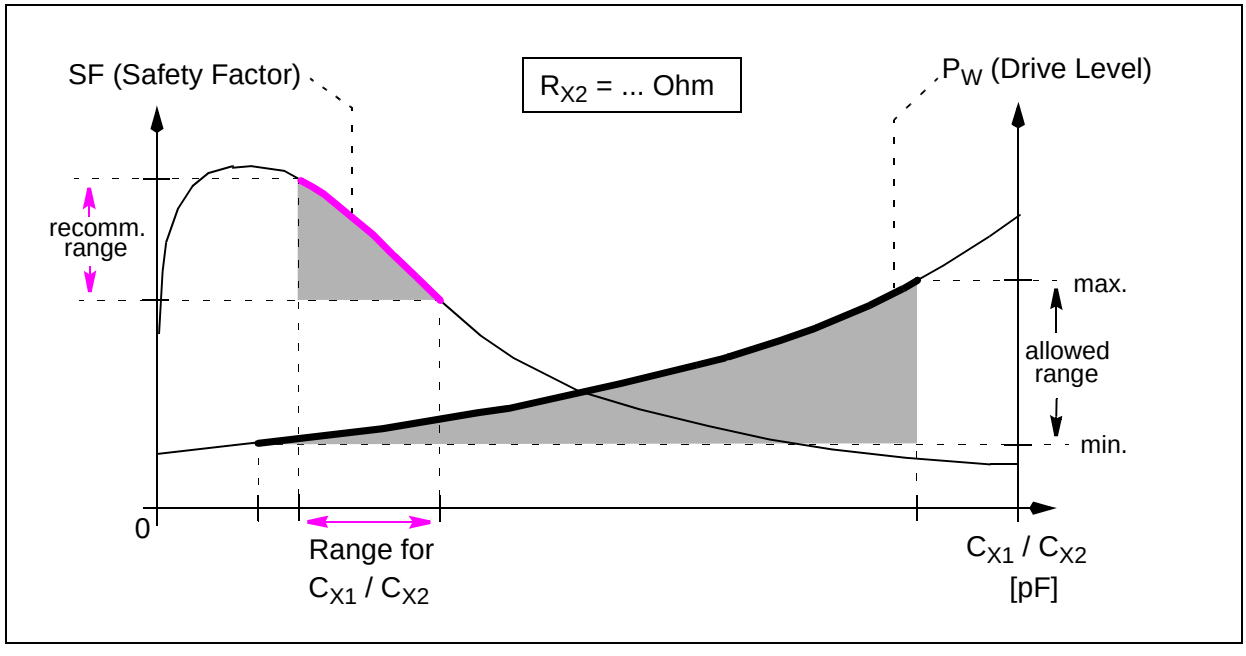

Figure 5 Evaluation Diagram for C_{X1} and C_{X2}

7 Oscillator Circuit Layout Recommendations

The layout of the oscillator circuit is important for the RF and EMC behavior of the design. The following recommendations can help to reduce problems caused by suboptimal layouts. This design recommendation is optimized for EMC (Electromagnetic Compatibility) aspects.

7.1 Avoid Capacitive Coupling

Minimize the crosstalk between oscillator signals and other signals. Separate sensitive inputs from outputs with a high amplitude.

Note: The crosstalk between different layers also has to be analyzed.

7.2 Ground the Crystal Package Correctly

Connect the crystal package to the ground plane directly underneath the crystal and to the ground layer via an interlayer connection. This method has the following advantages:

- The crystal metal package reduces electromagnetic emissions.
- The oscillating circuit's immunity to interference will be increased.
- The mechanical stability of the crystal is increased.

The ground layer and the additional ground plane underneath the crystal shield the oscillator. This shielding decouples all signals on the other side of the PCB.

7.3 Avoid Parallel Traces for High Frequency Signals

In order to reduce crosstalk caused by capacitive or inductive coupling, tracks for high frequency signals should not be routed in parallel (also not on different layers!).

7.4 Minimize Ground Supply Impedance

The ground supply must have a low impedance. The impedance can be reduced by using thick and wide ground tracks. Avoid ground loops because they can act as antennas.

Note: The connection to the ground should be done with a top-pin-clip because the heat of soldering can damage the quartz crystal.

7.5 Avoid Interference from Other Modules

Other RF modules should not be placed near the oscillator circuit in order to prevent them from influencing the crystal's operation.

7.6 Layout Example

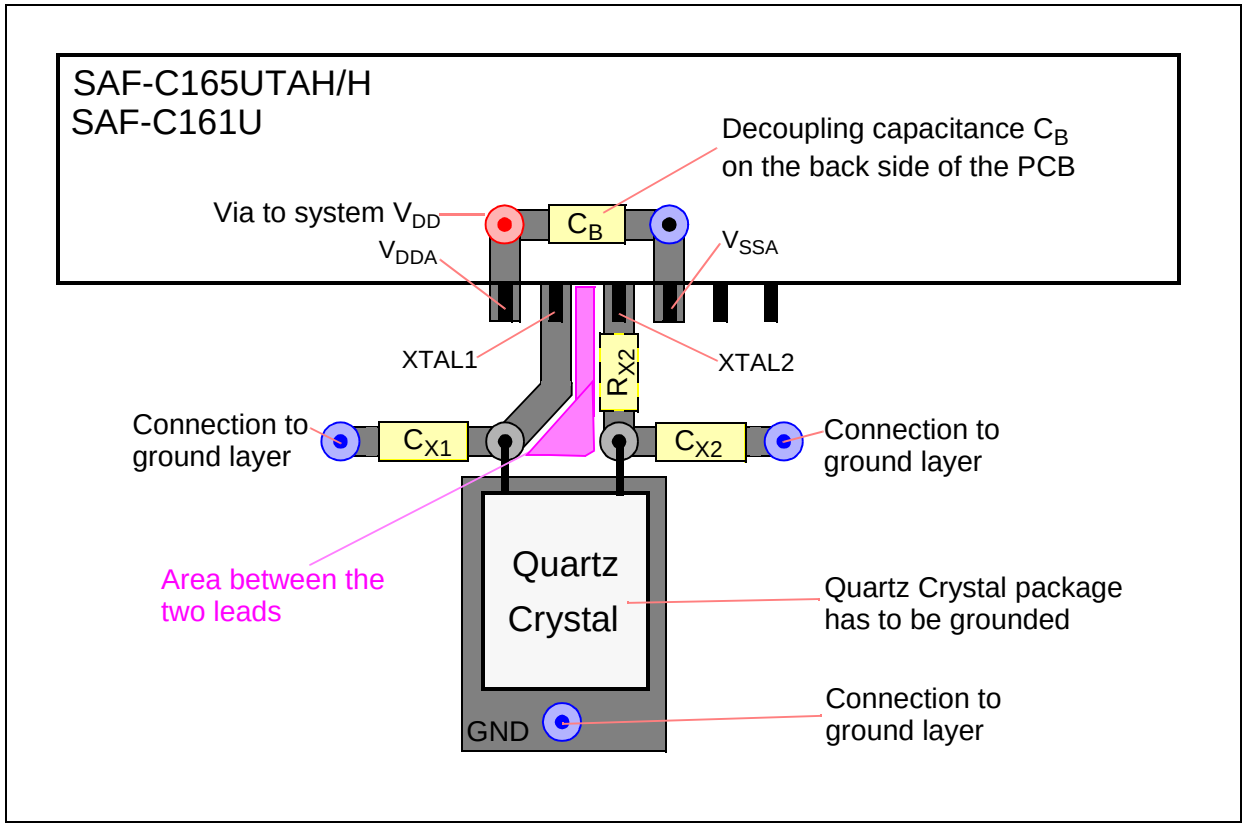

Figure 6 Layout Example for a Leaded Quartz Crystal

Note: The area built by the leads to the quartz crystal should be as small as possible. Therefore, the two leads should be as close as possible. This is essential to maximize the whole oscillating circuit's immunity to interference.

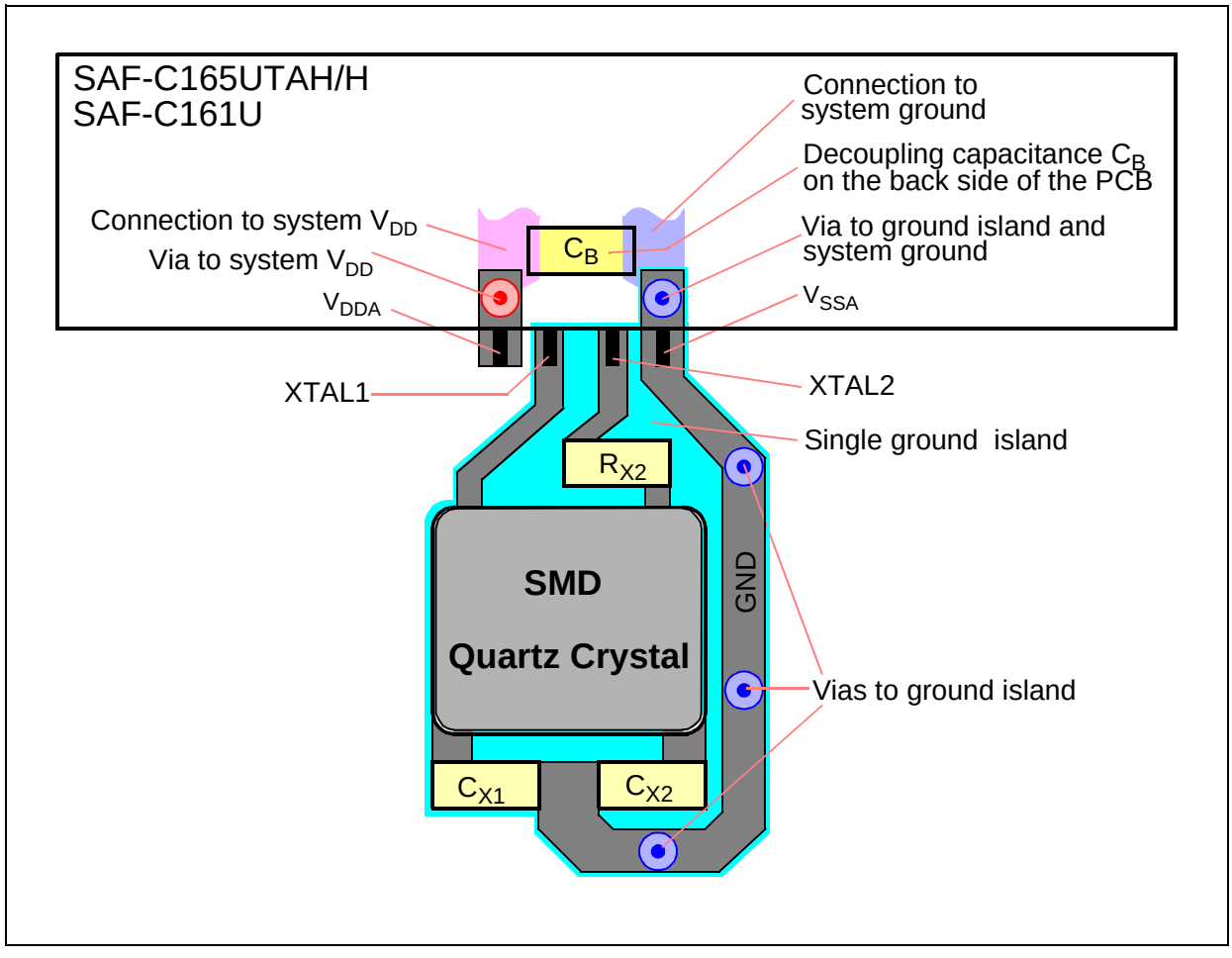

Figure 7 Layout Example for an SMD Quartz Crystal

Note: The interference immunity of the oscillating circuit can be reduced by using unshielded quartz crystals. Therefore, electromagnetic compatibility (EMC) tests (e.g., according to EN61000-4-2) should be done in an early development phase in order to find out if the proposed crystal is suitable for the application.

8 Glossary

C_0: Shunt capacitance of the quartz crystal (static capacitance)

C_{0typ}: Typical value of the shunt capacitance of the quartz crystal

C_1: Motional capacitance of the quartz crystal (dynamic capacitance)
Mechanical equivalent is the elasticity of the quartz crystal hardware blank

C_{1typ}: Typical value of the motional capacitance of the quartz crystal

C_L: Load capacitance of the system resp. quartz crystal

C_S: Stray capacitance of the system

C_{X1}, C_{X2}: Load capacitors

C_X: Capacitance to suppress bias voltage at XTAL2 output

C_{X2rest}: Capacitance of C_{X2} in combination with L_X in 3rd overtone mode

C_B: Decoupling capacitance for V_{DD} and V_{SS} on the Printed Circuit Board (PCB)
Depending on the EMC behavior, the value should be 22 -100 nF

f_{LXCX2}: Parallel resonance frequency of L_X and C_{X2}

f_{3rd}: Frequency of the 3rd overtone

f_{fund}: Frequency of the fundamental mode

I_{pp}: Peak-to-peak value of the quartz crystal current

I_Q: Drive current

L_1: Motional inductance of the quartz crystal (dynamic inductance).
Mechanical equivalent is the oscillating mass of the quartz crystal hardware blank

L_X: Inductance for 3rd overtone mode

$L_{Q:}$ Effective reactance

P_W: Drive level

Q: Quartz crystal

R_1, R_r: Series resistance of the quartz crystal (resonance resistance); in other technical descriptions also called: “Equivalent Series Resistance, ESR” or “transformed series resistance”). Mechanical equivalent is the molecular friction, the damping by mechanical mounting system and accustical damping by the gas-filled housing

R_{1typ} : Typical value of the series resistance at room temperature

R_{1max}: Maximum value of the series resistance at room temperature

R_{1max} (TK): Maximum value of the series resistance at the specified temperature range.
This value is the base for calculation of the SF in this application note

R_{Ltyp}, R_{Lmax}: Typical and maximum load resonance resistor (in other technical descriptions, also called “effective resistance”). R_L is the resistance of the quartz crystal at oscillating frequency and creates the power dissipation

R_Q: Test resistor for calculation of safety level

R_{Qmax}: Maximum value of the test resistor that does not stop the oscillation

R_{X2}: Resistor that controls the drive level (damping resistor)

SF: Safety Factor

t_{st_up}: Start-up time of the oscillator

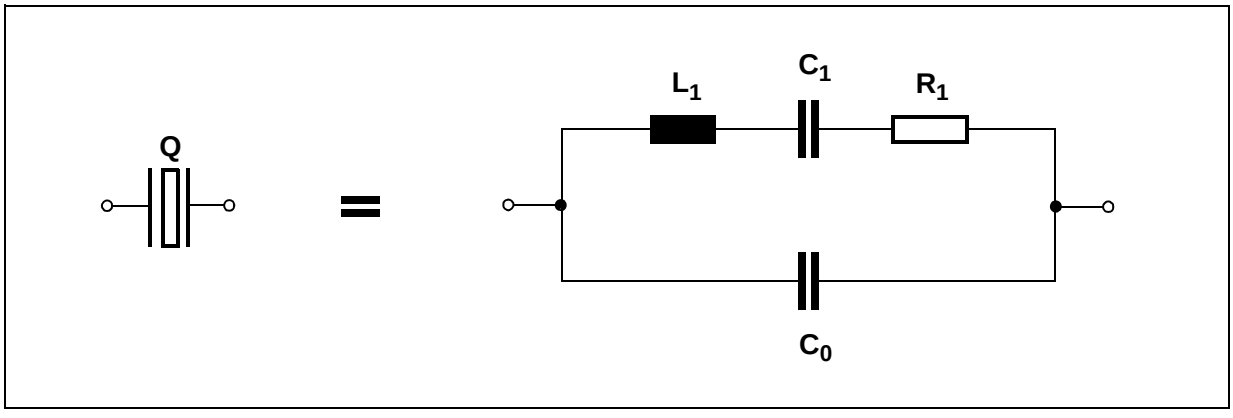

Figure 8 Equivalent Circuit of a Quartz Crystal

9 Recommended Start Values

The values mentioned below in table 4 should be regarded as start values for safety factor determination. **They do not release the system designer from a verification in the original system**  . It is mandatory to perform own investigations concerning the safety factor to get a problem-free operation of the oscillator. This is necessary because every design has a specific influence on the oscillator (noise, layout etc.).

Table 4 Start Values for Fundamental Mode

Fundamental Mode			
Frequency [MHz]	External Circuits		
	R_{X2} [Ω]	C_{X1} [pF] (Input)	C_{X2} [pF] (Output)
4.0	0	15	33
8.0	0	12	27
12.0	0	10	22
16.0	0	8.2	18
20.0	0	6.8	15

10 Useful Links

Crystal Manufacturers:

Telequarz Group	http://www.telequarz.de/
NDK	http://www.ndk-j.co.jp/
Murata	http://www.iijnet.or.jp/murata/
Kyocera	http://www.kyocera.co/jp/

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