YMPC-3001

Single Chip MP3 Encoder/Decoder

Preliminary Data sheet YDOC-3001

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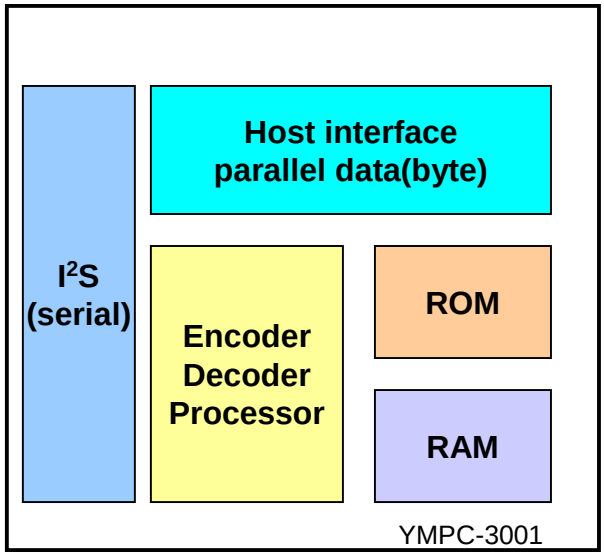
1. Introduction

YMPC-3001 is a single chip MP3 encoder/decoder with voice recorder. And MP3 encoder takes the digital audio input data through the I^2S interface.And the encoder will generate the compressed audio data in MP3 format and this chip will compute the ECC bits per one frame. This feature will be useful for external SMC writing. The Decoder part will get the MP3 data from the SMC or flash memory and decode the MP3 data into PCM bit stream.



General Features

- 3.3 V Operation
- Serial Audio data input
- Parallel host interface (byte)
- ECC generation for encoder
- Power consumption:
  - Encoder:85mA(Nominal Mode)
  - Decoder:40 mA(Nominal Mode)
  - Power down:100 uA(stop mode)
- 144 pin TQFP

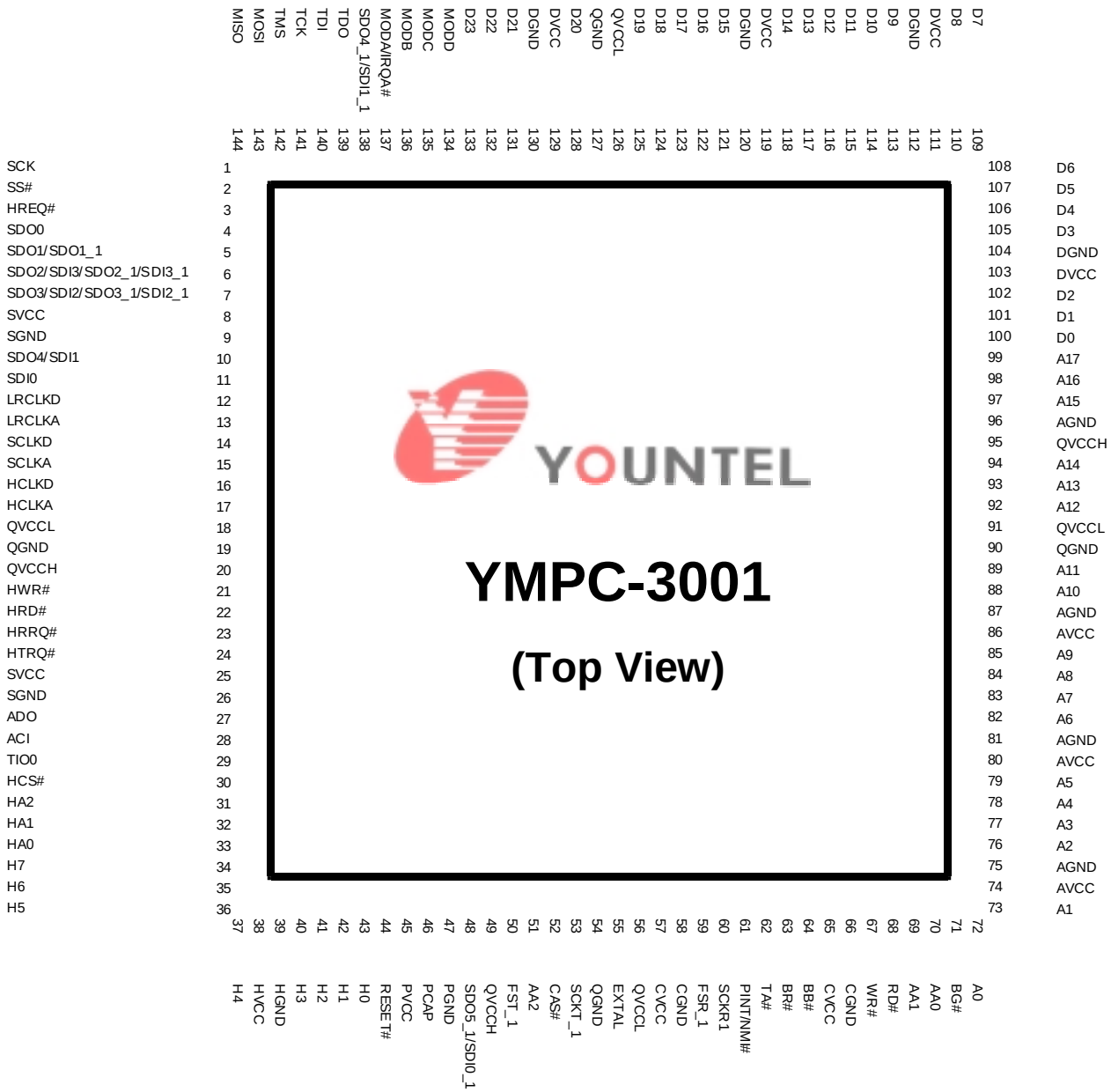
Encoder

- Music :
  24 bit , 44.1khz sampled data Input
  128kbps joint-stereo MP3 data output
- Voice:
  24 bit ,16 kHz sampled data input
  16kbps ,mono MP3 data output.

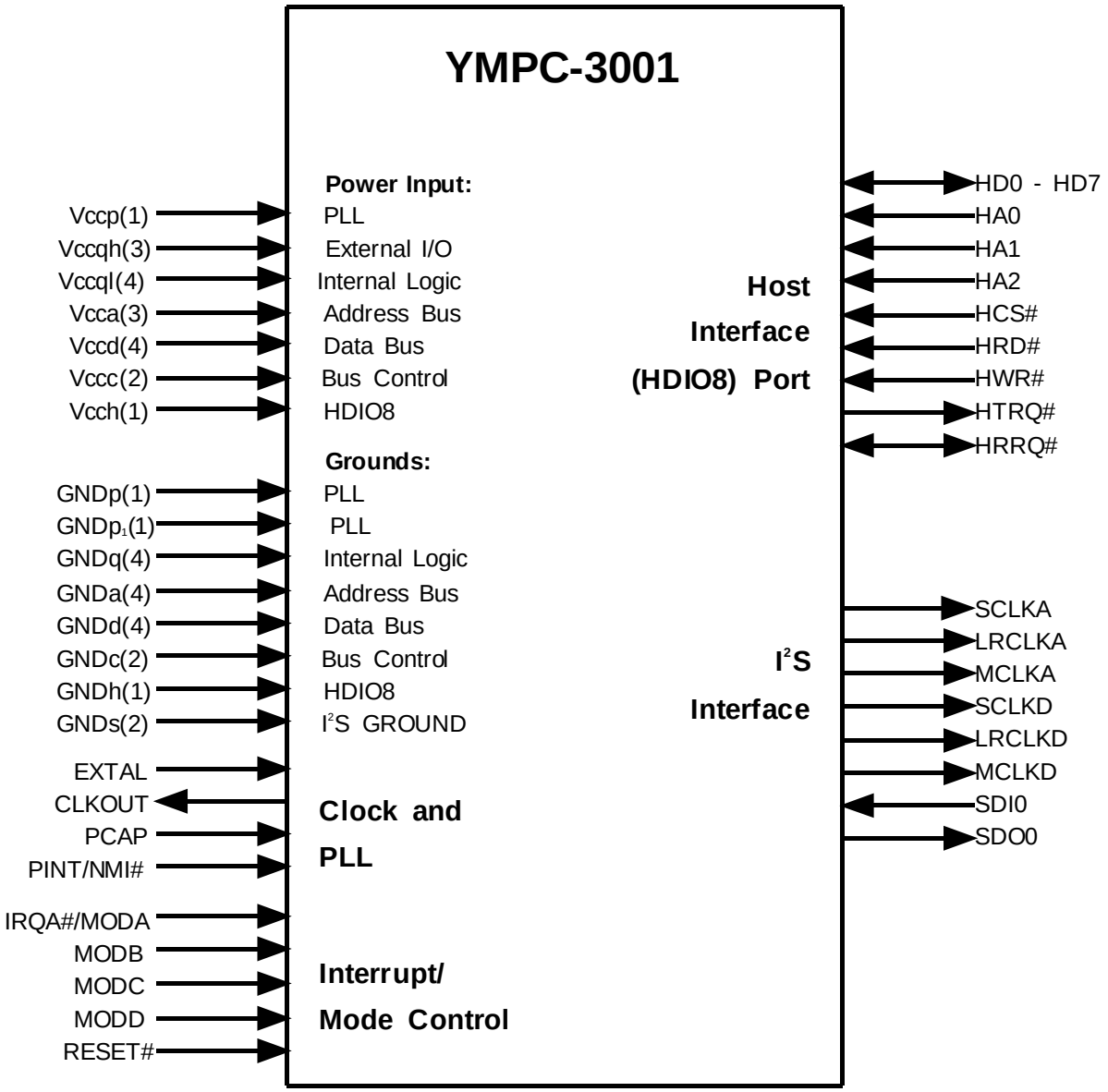
Decoder

- Music:
  MPEG1 layer3 ,MPEG2 layer3
  bit stream decoding.
- Voice:
  24 bit ,16kbps decoding .

2. Pin description and connection



PIN CONNECTION DIAGRAM



Power Supplies

Power Name	Description
Vccp	**PLL Power**-Vccp is Vcc dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the Vcc power rail. There is one Vccp input.
Vccql(4)	**Quiet Core (Low) Power-**Vccql is an isolated power for the core processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four Vccql inputs.
Vccqh(3)	**Quiet External (High) Power**-Vccqh is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three Vccqh inputs.
Vcca(3)	**Address Bus Power** - Vcca is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three Vcca inputs.
Vccd(4)	**Data Bus Power** - Vccd is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four Vccd inputs.
Vccc(2)	**Bus Control Power** - Vccc is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two Vccc inputs.
Vcch	**Host Power** - Vcch is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one Vcch input.
Vccs(2)	**I^2S Serial port Power** - Vccs is an isolated power for I^2S Serial port I/O drivers. This input must be tied externally to all other chip power inputs . The user must provide adequate external decoupling capacitors. There are two Vccs inputs.

Grounds

Power Name	Description
GNDp	**PLL Ground** - GNDp is ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. Vccp should be bypassed to GNDp by a 0.47 uF capacitor located as close as possible to the chip package. There is one GNDp connection.
GNDp1	**PLL Ground 1** - GNDp1 is ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. There is one GNDp1 connection.
GNDq(4)	**Quiet Ground** - GNDq is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GNDq connections.
GNDa(4)	**Address Bus Ground** - GNDa is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GNDa connections.
GNDd(4)	**Data Bus Ground -** GNDd is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GNDd connections.
GNDc(2)	**Bus Control Ground** - GNDc is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GNDc connections.
GNDh	**Host Ground** - GNDh is an isolated ground for the HDI08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GNDh connection.
GNDs(2)	**I^2S serial ports Ground** - GNDs is an isolated ground for the I^2S serial ports I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GNDs connections.

Clock and PLL

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input** - An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
PCAP	Input	Input	**PLL Capacitor** - PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to Vccp. If the PLL is not used, PCAP may be tied to Vcc, GND, or left floating.
PINIT/ NMI#	Input	Input	**PLL Initial/Nonmaskable Interrupt** - During assertion of RESET, the value of PINIT/NMI is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After RESET deassertion and during normal instruction processing, the PINIT/NMI Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to CLKOUT. PINIT/NMI# **cannot** tolerate 5 V.

Interrupt/Mode control

Signal Name	Type	State during Reset	Signal Description
MODA/ IRQA#	Input	Input	**Mode Select A/External Interrupt Request A -** MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal processing. MODA, MODB, MODC, and MODD select one of 3 initial chip operating modes, latched into an internal register when the RESET signal is deasserted. If IRQA# is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting IRQA# to exit the wait state. If the YMPC-3001 is in the stop standby state and IRQA# is asserted, the YMPC-3001 will exit the stop state. *This input is 5 V tolerant.*
MODB	Input	Input	**Mode Select B** - MODB is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 3 initial chip operating modes, latched into a register when the RESET signal is deasserted. *This input is 5 V tolerant.*
MODC	Input	Input	**Mode Select C -** MODC is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 3 initial chip operating modes, latched into a register when the RESET signal is deasserted. *This input is 5 V tolerant.*

Interrupt/Mode control (continued)

Signal Name	Type	State during Reset	Signal Description
MODD	Input	Input	**Mode Select D** - MODD is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODD selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 3 initial chip operating modes, latched into OMR when the RESET signal is deasserted. *This input is 5 V tolerant.*
RESET#	Input	Input	**Reset -** RESET is an active-low, Schmitt-trigger input. Deassertion of RESET is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If RESET is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in "lock-step." When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted after power up. *This input is 5 V tolerant.*

Operating Mode

Mode	MODD	MODC	MODB	MODA	Reset Vector	Description
1	0	0	0	1	$FF0000	Bootstrap from byte-wide memory
2	0	0	1	0	$FF0000	Jump to PROM starting address
3	1	1	0	1	$FF0000	HDI08 Bootstrap in HC11 non-multiplexed mode

Host Interface Bus

Signal Name	Type	State during Reset	Signal Description
H0 - H7	Input/ output	GPIO disconnected	**Host Data** - The HDI08 is to interface a nonmultiplexed host bus an, these signals are lines 0~7 of the data bidirectional, tri-state bus. *This input is 5 V tolerant.*
HA0	Input	GPIO disconnected	**Host Address Input 0** - The HDI08 is to interface a nonmultiplexed host bus and , this signal is line 0 of the host address input bus. *This input is 5 V tolerant.*
HA1	Input	GPIO disconnected	**Host Address Input 1** - The HDI08 is to interface a nonmultiplexed host bus and , this signal is line 1 of the host address (HA1) input bus. *This input is 5 V tolerant.*
HA2	Input	GPIO disconnected	**Host Address Input 2** - The HDI08 is to interface a non-multiplexed host bus and this signal is line 2 of the host address (HA2) input bus. *This input is 5 V tolerant.*
HRD#	Input	GPIO disconnected	**Host Read Data** - This signal is the host read data strobe (HRD#) Schmitt-trigger input. The polarity of the data strobe is configured as active-low (HRD#) after reset. *This input is 5 V tolerant.*
HWR#	Input	GPIO disconnected	**Host Write Data** - This signal is the host write data strobe (HWR#) Schmitt-trigger input. The polarity of the data strobe is configured as active-low (HWR#) following reset. *This input is 5 V tolerant.*

Host Interface Bus (continued)

Signal Name	Type	State during Reset	Signal Description
HCS#	Input	disconnected	**Host Chip Select -** This signal is the host chip select (HCS) input. The polarity of the chip select is configured active-low (HCS) after reset. *This input is 5 V tolerant.*
HTRQ#	Output	disconnected	**Transmit Host Request -** this signal is the transmit host request (HTRQ#) output. The polarity of the host request is configured as active-low(HTRQ#) following reset.
HRRQ#	Output	disconnected	**Receive Host Request** - this signal is the receive host request (HRRQ#) output. The polarity of the host request is configured as active-low(HRRQ#) after reset.

I²S BUS Interface

Signal Name	Type	State during Reset	Signal Description
MCLKA	output	disconnected	**Master Clock for A/DC** - This signal serves as a high-frequency master clock for external analog to digital converters [ADCs]. *.MCLK=256 fs* Note) when a codec is used , MCLKA and MCLKD are tied up together to supply the MASTER Clock to the CODEC chip
MCLKD	output	disconnected	**Master Clock for D/AC** - This signal serves as a high frequency master clock for external digital to analog converters [DACs]. *MCLK=256fs* Note) when a codec is used , MCLKA and MCLKD are tied up together to supply the MASTER Clock to the CODEC chip.
LRCLKA	output	disconnected	**LRCLK for A/DC** - This is the receiver frame sync output signal. This signal serves as a Left/Right CH frame sync clock for external analog to digital converters [ADCs]. *LRCLKA=fs*

I²S BUS Interface (continued)

Signal Name	Type	State during Reset	Signal Description
LRCLKD	output	disconnected	**LRCLK for D/AC** - This signal serves as a Left / Right CH frame sync clock for external I²S digital to analog converters [DACs]. *LRCLKD=fs*
SCLKA	output	disconnected	**Serial Clock for A/DC** - SCLKA provides the serial bit clock for the I²S type A/D converters. *SCLKA=64fs*
SCLKD	output	disconnected	**Serial Clock for D/AC** - This signal provides the serial bit rate clock for the I²S type D/A converters. *SCLKD=64fs*
SDI0	Input	disconnected	**Serial Data Input 0 from A/DC** - SDI0 is used to receive serial data into the internal serial receive shift register. *This input is 5 V tolerant.*
SDO0	Output	disconnected	**Serial Data Output 0 to D/AC** - SDO0 is used to transmit data from the internal serial transmit shift register.

3. A/D Converter Interface

YMPC-3001 has two I^2S interface bus , one is for audio input and the other is for audio output .
In order to make an interface between A/D converter and YMPC-3001 ,you can read this section and just follow the direction .
In the section 1 , you can find the pin descriptions that you need to know to proceed this section.

3-1 Selection of A/D converters .

-A/D C must have over 20 bits/sample data resolution .
-The data interface should be I^2S compatible serial format.
- Sampling frequency :16Khz , 44.1Khz(fs)
16Khz sampling is used for voice recording , and 44.1khz sampling for music recording.

3-2 Connection of the related pins

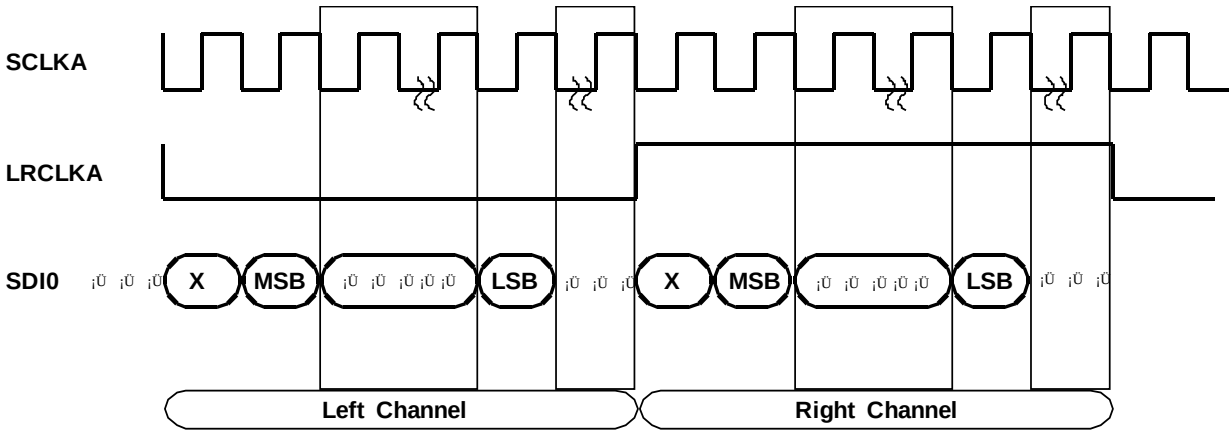
-SDI0 : receives A/D converted audio serial bit stream --connected to A/DC output .
-LRCLKA: generates Left/Right CH synchronization Clock (fs)- connected to A/DC LRCLK .
-SCLKA : generates a serial clock(64fs) to fetch the serial audio data from A/D - connected A/DC serial clock input port.
-MCLKA: this port generate a master clock($256f_{S)}$ to be supplied for A/D converter.

3-3 A/DC interface consideration .

The ADC performance affects the final sound quality seriously.
Especially , the analog front-end circuits should be designed carefully according to the vendors recommendation .
There are some factors that you have to pay attention to .
They are the SNR , Dynamic range and THD . and so on .
We recommend the SNR over 85 dB , Dynamic Range over 85 dB .
and the THD figure is less than 0.003 % .

3-4 Operation (I²S -Compatible Serial Format for 24 bits)

Left channel data is valid when LRCLKA is LOW.
SDI0 is sampled with the falling edge of SCLKA.



4.D/A Converter Interface

YMPC-3001 has a serial audio data output for D/A converter

4-1 Selection of D/A converters .

-D/A C must have over 16 bits/sample data resolution .
-The data interface should be I²S compatible serial format.
- Sampling frequency :16Khz~48Khz(fs)

4-2 The related Pins are as follows :

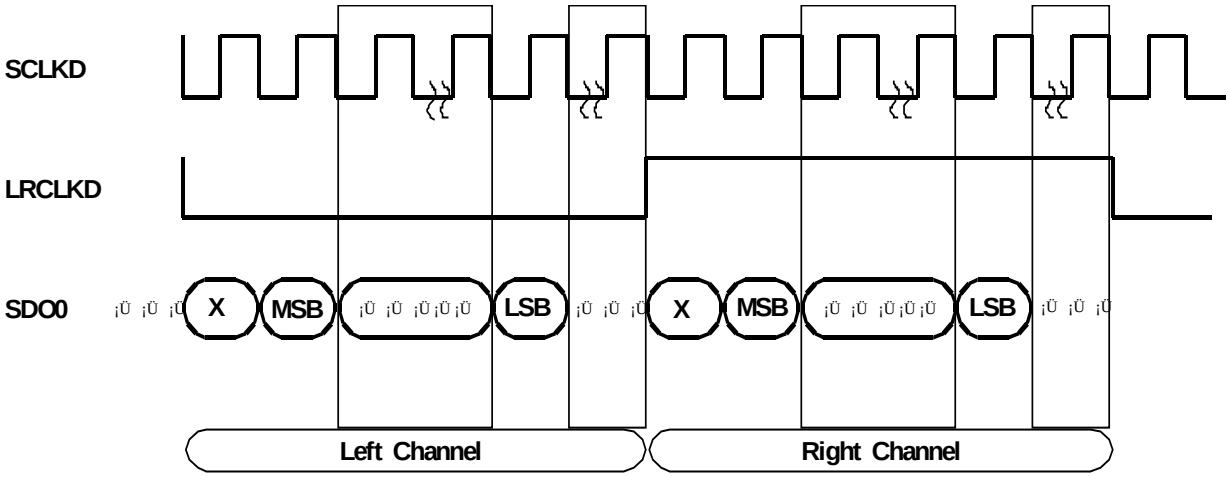
-SCLKD : generates Serial clock to transmit digital audio data bits to D/AC
SCLK rate is varying according to the audio bit stream bit rate .
-LRCLKD : generates Left ,right CH synchronization clock for D/AC
LRCLK rate is directly proportional to SCLKD varying as 64SCLKD .
-SDO0 : Digital audio output for D/A converter(connected to D/A input).
-MCLKD : MCLKD is 256 f_s rate clock for D/A master clock .

4-3 D/AC interface consideration

The ADC performance affects the final sound quality seriously.
Especially , the analog front-end circuits should be designed carefully according to the vendors recommendation .
There are some factors that you have to pay attention to .
They are the SNR , Dynamic range and THD . and so on .
We recommend the SNR over 85 dB , Dynamic Range over 85 dB .
and the THD figure is less than 0.003 % .

4-4 Operation

Left channel data is valid when LRCLKD is low .
Audio data bit on SDO0 is transmitted on rising edge of SCLKD.



5.Host controller Interface

5-1. Interface lines between YMPC-3001 and host controller

In order to make a MP3 Recorder/Player , YMPC_3001 requires a host controller. The Host controller will communicate with YMPC-3001 through the host interface bus , which is show in the table below .
And you may choose a 8bit or 16 bit single chip micro-controller as Host controller according to your application product.

- TOTAL : 17 LINE

PIN	Function	I/O	Remark
RESET#	YMPC-3001 CHIP RESET	INPUT	Host controller is working as a MASTER
HCS#	CHIP SELECT	INPUT	
HWR#	WRITE ENABLE	INPUT	
HRD#	READ ENABLE	INPUT	
HTRQ#	DATA RECEIVER READY	OUTPUT	
HA2-0	ADDRESS LINE (3 LINE)	INPUT	
H7-0	DATA LINE (8 LINE)	Bi-direction	
IRQA#	YMPC-3001 POWER SAVE MODE DISABLE	INPUT	

5-2. Terminology

1) ADDRESS

- ICR	(Interface Control)	: 0x00
- CVR	(Command Vector)	: 0x01
- ISR	(Interface Status)	: 0x02
- IVR	(Interrupt Vector)	: 0x03
- RXH	(Receive Data High Byte)	: 0x05
- RXM	(Receive Data Middle Byte)	: 0x06
- RXL	(Receive Data Low Byte)	: 0x07
- TXH	(Transmit Data High Byte)	: 0x05
- TXM	(Transmit Data Middle Byte)	: 0x06
- TXL	(Transmit Data Low Byte)	: 0x07

2) DATA

- DSP_MP3ENC	(DATA transmission method)	: 0x01
- COMVEC_ENC_START	(Encoding Start COMMAND)	: 0xB2
- COMVEC_STOP	(Encoding/Decoding /Voice STOP)	: 0xB3
- COMVEC_DEC_START	(Decoding START)	: 0xB4
- COMVEC_PODON	(DSP Power Down MODE)	: 0xB6
- COMVEC_SYNC_ON	(SYNC Encoding ON)	: 0xB7
- COMVEC_SYNC_OFF	(SYNC Encoding OFF)	: 0xB8
- COMVEC_TRK_CHG	(Track Change)	: 0xB9
- COMVEC_NOM_VOI_START	(Normal Voice Encoding START)	: 0xB5
- COMVEC_LON_VOI_START	(Long Voice Encoding START)	: 0xBB
- COMVEC_EQ_OFF	(DIGITAL EQ OFF COMMAND)	: 0xC0
- COMVEC_EQ_JAZ	(DIGITAL EQ JAZZ ON COMMAND))	: 0xC1
- COMVEC_EQ_CLA	(DIGITAL EQ CLASSIC ON COMMAND))	: 0xC2
- COMVEC_EQ_TEC	(DIGITAL EQ TECHNO ON COMMAND))	: 0xC3
- COMVEC_EQ_POP	(DIGITAL EQ POP ON COMMAND))	: 0xC4
- COMVEC_EQ_ROC	(DIGITAL EQ ROCK ON COMMAND))	: 0xC5
- COMVEC_DIG_BASS	(DIGITAL BASS ON COMMAND))	: 0xC8
- COMVEC_DIG_OFF	(DIGITAL BASS OFF COMMAND))	: 0xC9

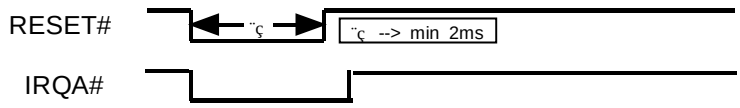
5-3. YMPC-3001 Functions and Host controller Interface Timing

YMPC-3001 initial boot-up mode selection

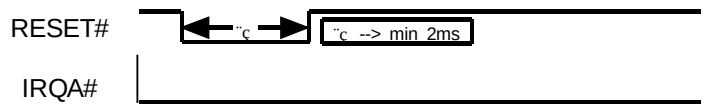
Operation MODE	MODE				Description
	MOD D	MOD C	MOD B	MODA (IRQA)	
Self boot-up mode	0	0	1	0	YMPC-3001 internal boot up
EPROM boot-up mode	0	0	0	1	EPROM boot up - 1.downloading the code from EPROM to YMPC-3001 internal ram area . 2.then Start to run the downloaded code.
Host controller boot-up mode	1	1	0	0	Host controller boot up - Host controller can have some code to run in YMPC-3001 then host controller can send the program code to YMPC-3001 by using HDI08 and start to run the code.

5-4 Operation after power-on

Self boot-up mode :
Host controller will reset YMPC-3001 at the POWER-ON ,supplying logical Low on the IRQA# port.
And also keeping RESET# port in active Low for more than 2msec after then release IRQA# to high.



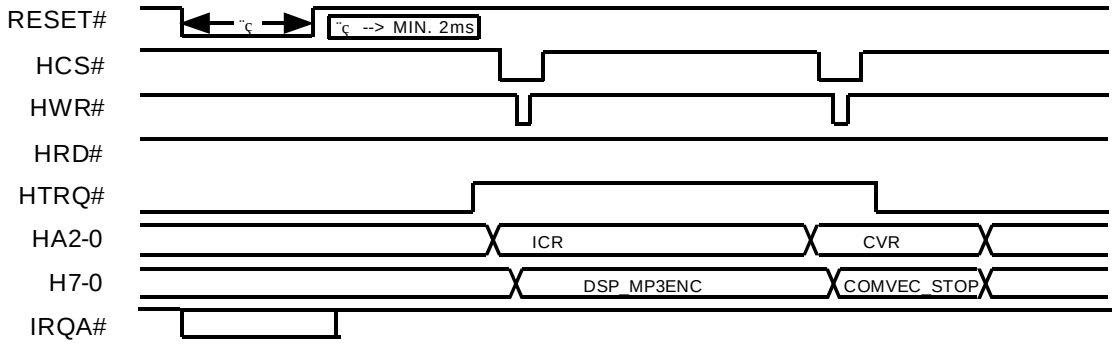
EPROM or Host controller boot-up mode :
Host controller will reset YMPC-3001 at the POWER-ON ,Supplying logical Low on IRQA# port.
And also keeping RESET# port in active Low for more than 2ms .



5-5 Initial Operation and its Timing after RESET

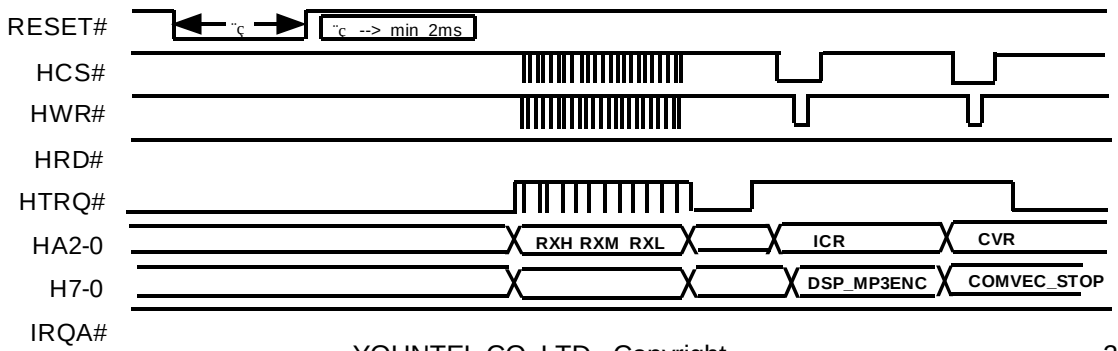
In the EPROM or Self Boot-Up mode

After RESET , YMPC-3001 will initialize the internal memory and registers and so on, then YMPC-3001 will set HTRQ# Hi to get command from Host controller.
When the HTRQ# is HIGH,Host controller will generate the output on the host interface ports as ADD=ICR, DATA=DSP_MP3ENC(DATA transmission method) and 10ms later , host controller will alter the outputs as ADD=CVR, DATA=COMVEC_STOP(YMPC-3001 initialization complete)



In the Host controller Boot-Up MODE

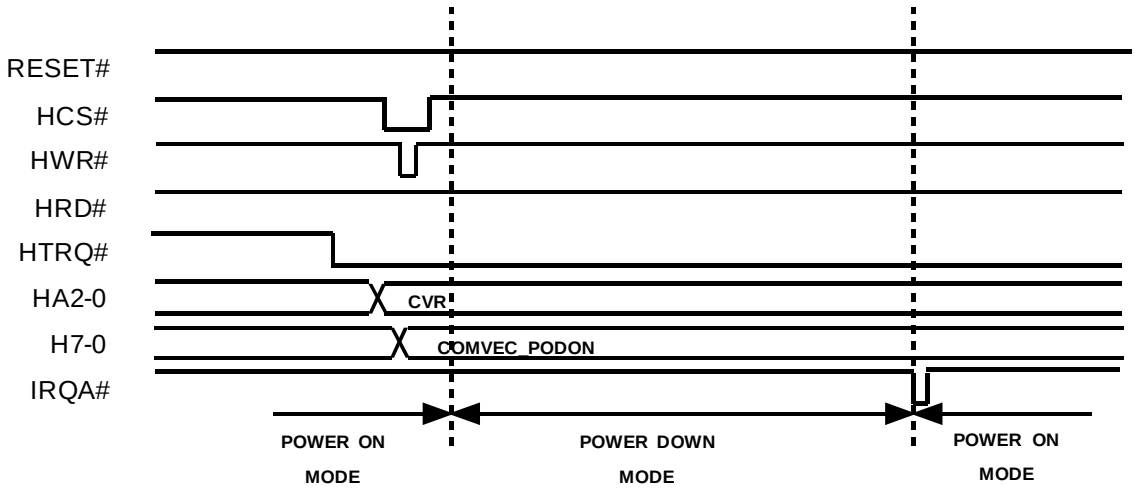
After reset , YMPC-3001 will alter the HTRQ# to Hi to get data from host controller
When HTRQ# is HIGH, Host controller transmit the program code to YMPC-3001 .
After downloading the program code ,YMPC-3001 will initialize the internal memory and set ready Hi to get data from host controller.
When Ready is Hi ,Host controller will alter the host interface ports as ADD=ICR, DATA=DSP_MP3ENC(DATA transmission method).
And 10ms later , host controller will alter the ports as ADD=CVR, DATA=COMVEC_STOP(DSP initialization complete).



5-6 POWER DOWN MODE

Setting YMPC-3001 POWER DOWN MODE
When YMPC-3001 is in idle state for a certain period,host controller can make YMPC-3001to be in POWER DOWN MODE by sending a command , COMVEC_PODON (DSP POWER DOWN MODE command) to YMPC-3001.
YMPC-3001 then enter the POWER DOWN MODE and stop supplying power to the PORTs which consume power.

Releasing YMPC-3001 from POWER DOWN MODE
To release YMPC-3001 from POWER DOWN MODE , Just keep IRQA# LOW for 1uS .



5-7 ENCODING

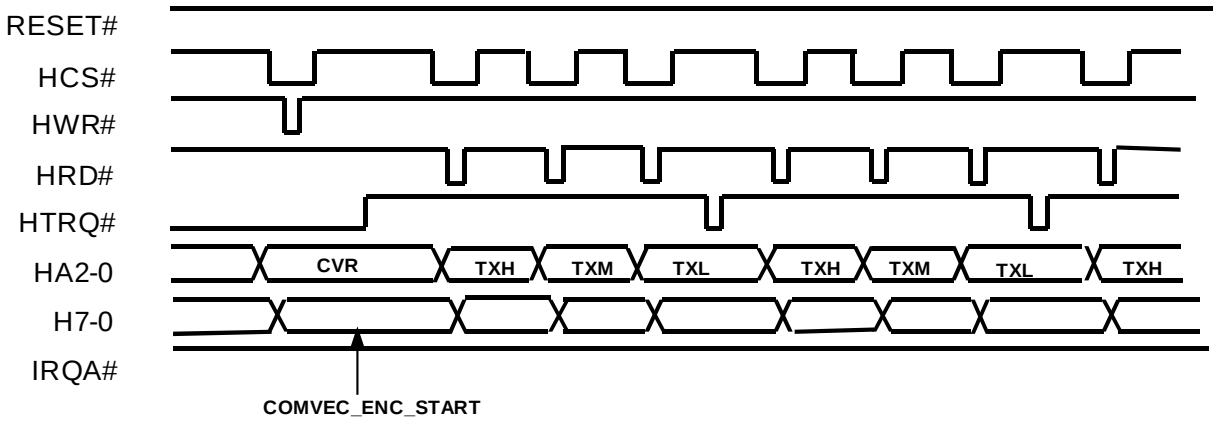
GENERAL ENCODING FUNCTIONS

Encoding Functions
Encoding sources : MUSIC, VOICE
Encoding methods: Continuous Recording , SYNC Recording .

Conditions for ENCODING Operation .
Encoding can begin when the system is in the STOP STATUS.
While the recording of music,the transition between continuous and sync recording is allowed.
Initial status on RESET : Music, continuous recording mode.
VOICE ENCODING can begin on the STOP status, VOICE ENCODING type can be modified only on the STOP status.

Continuous MUSIC ENCODING

Encoding Operation
Host controller will transmit the command to YMPC-3001 to start encoding :
ENCODING START COMMAND ADD=CVR, DATA=COMVEC_ENC_START
Then YMPC-3001 will start encoding and when it is ready to transmit
the encoded data to host controller , it will alter the HTRQ# to HI.
When the HTRQ# is HIGH, the HOST Controller will receive the data in the order as HIGH, MIDDLE, LOW BYTE .



Data transmission of continuous music encoding

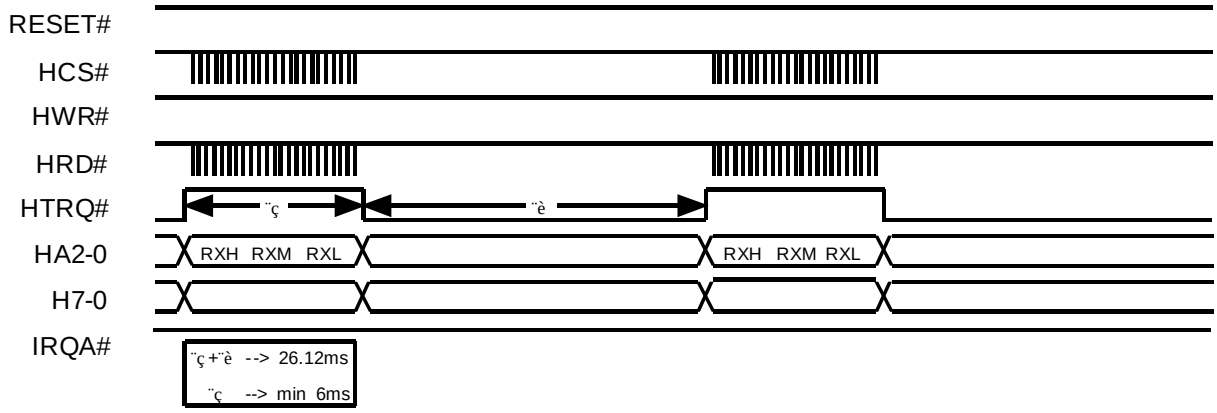
Once started encoding , YMPC-3001 transmits the encoded DATA to host controller.
Where the pure encoded data size is 512 bytes per a block .

YMPC-3001 is encoding the input bit stream by FRAME(26.12mS) , and When the encoded data size is over than 512 bytes , it will generates 6 bytes ECC for every 512 bytes data and the residue will be reserved for the next data block .
The current block to transmit will be made with 512 bytes of the encoded data and 16 bytes of spare area data including 6 bytes of ECC to make 528 bytes.
And the consistent data size to transmit to Host controller is 528bytes .

Note) Spare Area data structure for ENCODING (16Byte)

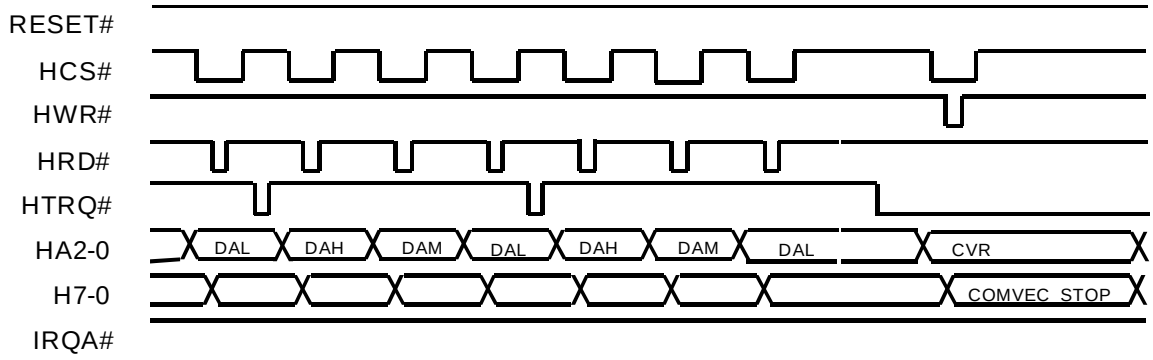
Byte No	Contents	data	Byte No	Contents	Data
512	User Data Area	FF	520	ECC Area -2	ECC Data of Area -2
513		FF	521		
514		FF	522		
515		FF	523	Block Address Area -2	FF
516	Data Status Flag	FF	524		FF
517	Block Status Flag	FF	525	ECC Area -1	ECC Data Area -1
518	Block Address Area -1	FF	526		
519		FF	527		

When the encoded DATA is less than 512bytes ,YMPC-3001 will not transmit the data and will keep the ready signal Low until the next frame encoded .



Continuous Music ENCODING Termination FLOW

When Host controller recognizes the completion of encoding , host controller will send STOP COMMAND to YMPC-3001 as ADD=CVR, DATA=COMVEC_STOP



Denoting the silence area(Sync period)
If the encoded data is silence the YMPC-3001 denotes the encoded frame as a silence (sync)period by writing the Spare Area Structure as below .
And if the Host controller keep receiving the silence patterns for over
2.5 sec, it will notice that the current encoded data belongs to the transition period between music titles and it will store the new frame under a new title.
After then, host controller will delete the 2.5 sec period of silence out of the previous title.

Byte No	Contents	data	Byte No	Contents	Data
512	User Data Area	FF	520	ECC Area -2	Area -2
513		00	521		ECC
514		00	522		Data
515		00	523	Block Address	FF
516	Data Status Flag	FF	524	Area -2	FF
517	Block Status Flag	FF	525	ECC Area -1	Area -1
518	Block Address	FF	526		ECC
519	Area -1	FF	527		Data

VOICE RECORDING

There are two modes(Normal, Sync) in VOICE ENCODING, and these modes can be selected only when system is in the STOP mode.

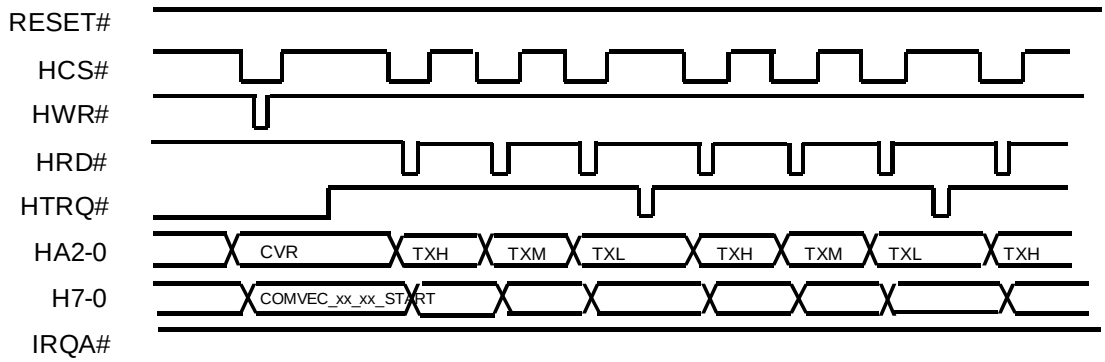
NORMAL VOICE Recording :
Normal VOICE ENCODING (16kbps)

Sync VOICE Recording :
In this mode,any silence period longer than t sec is fixed in t sec,
where t sec is 1 sec in default, and host controller can set a new value for t .

Voice Recording Flow

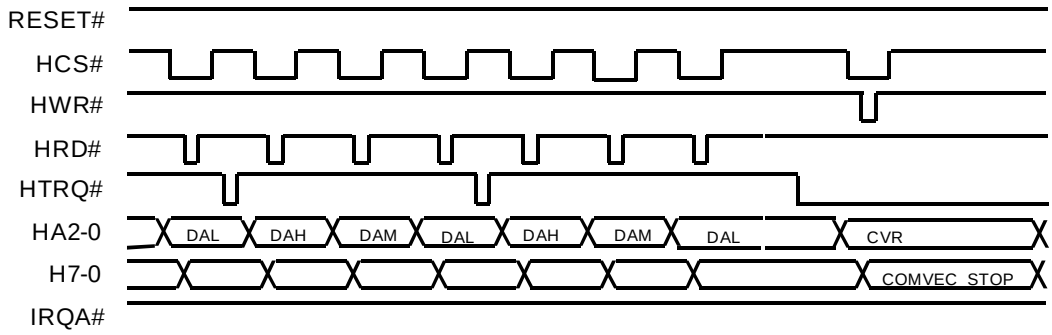
Host controller transmits the voice recording start command to YMPC-3001 when it is in the STOP mode.

START COMMAND :ADD=CVR, DATA=COMVEC_xx_xx_START



Voice Recording Termination Flow

After completion of voice data transmission (when HTRQ# is LOW),host controller will send the STOP COMMAND to YMPC-3001.STOP COMMAND: ADD=CVR, DATA=COMVEC_STOP.



5-8 DECODING

General Functions of DECODER

DECODER functions

-Normal MP3 DECODING

-DIGITAL EQUALIZER

Band	60Hz	170Hz	310Hz	600Hz	1KHz	3KHz	6KHz	12KHz	14KHz	16KHz
Classic	0.0	0.0	0.0	0.0	0.0	0.0	-7.2	-7.2	-7.2	-9.6
Jazz	9.6	7.5	4.1	0.0	0.0	-4.8	0.0	0.0	7.2	9.6
Pop	-1.6	4.8	7.2	8.0	5.6	0.0	-2.4	-2.4	-1.6	-1.6
Rock	0.0	4.8	-5.6	-8.0	-3.2	4.0	8.8	11.2	11.2	11.2
Techno	8.0	5.6	0.0	-5.6	-4.8	0.0	8.0	9.6	9.6	8.8

-DIGITAL BASS

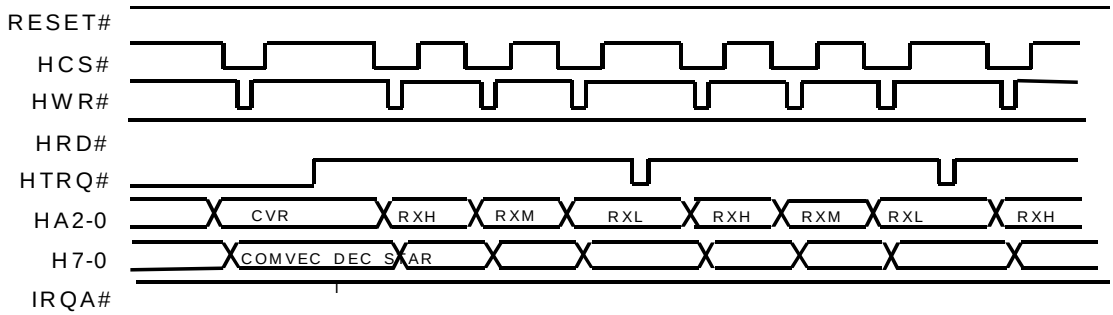
BAND	60Hz	170Hz	310Hz	600Hz	1KHz	3KHz	6KHz	12KHz	14KHz	16KHz
DIGITAL BASS	9.6	9.6	9.6	5.6	1.6	-2.0	-4.0	-5.2	-5.6	-5.6

Conditions for DECODER Operations
Decoder operation can start only when the system is in the STOP Mode.
Digital EQ or BASS can be selected in the midst of the decoder operation.

Decoding Operation

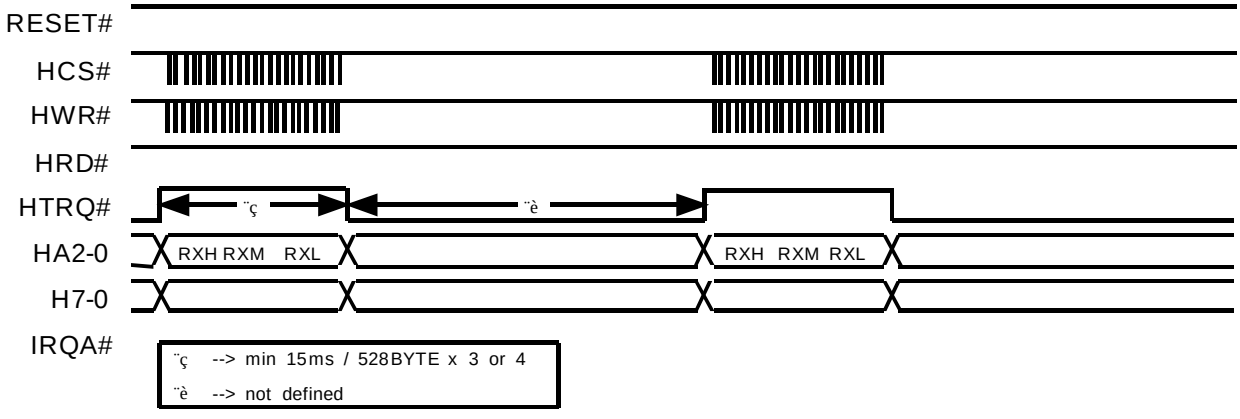
Decoding start flow

Host controller send a DECODING START COMMAND to YMPC-3001
as ADD=CVR, DATA=COMVEC_DEC_START.
Then YMPC-3001 will prepare to receive DATA to be decoded and when it is ready to receive data from host , it alters the ready signal HI.
Then host controller will transmit 4 or 3 blocks of 528bytes DATA to YMPC-3001.
The DATA is in the order of HIGH, MIDDLE, LOW BYTE.
※ Only for the first term of data transmission of a new title, 4 blocks of 528bytes DECODING DATA will be transmitted and after then normally 3 blocks of 528byts will be sent to YMPC-3001 until next title comes.



Receiving DATA from Host controller

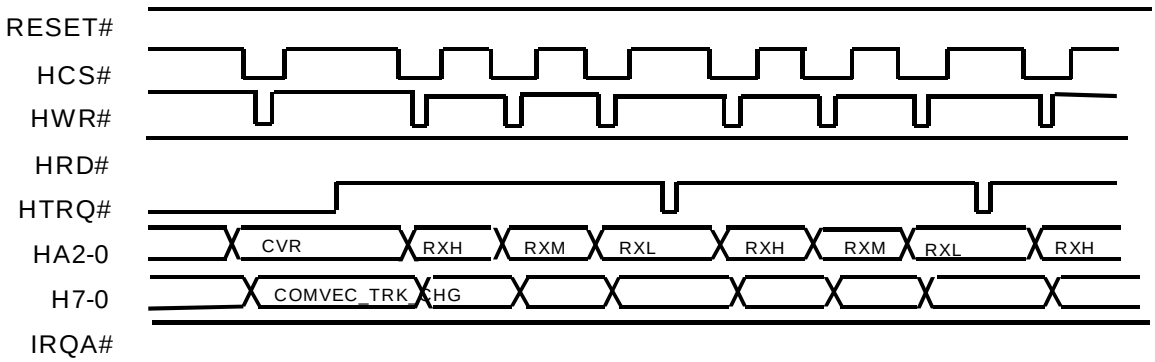
Once start decoding, Host will send 3 blocks of 528BYTE to YMPC-3001 as a unit.
(Except the first unit of the title is 528BYTE x 4)
While YMPC-3001 is decoding the data by FRAME(26.12mS)at a time and when it requires DATA to decode ,it will set HTRQ# signal HIGH and it will receive another DATA unit to decode from the host controller.



Decoding the next title

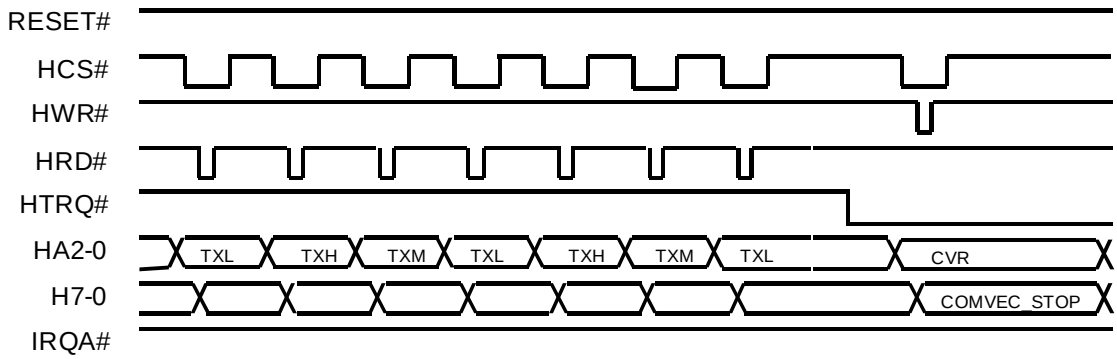
If host wants for YMPC-3001 to decode the other title , before it sends another Data unit to YMPC-3001,host will send a TRACK CHANGE COMMAND to YMPC-3001 as ADD=CVR,DATA=COMVEC_TRK_CHG.
YMPC-3001 will prepare to decode a new title ,and when it is ready , it will set the HTRQ# High.
When HTRQ# is HIGH,Host will send 4 blocks of 528BYTE DECODING DATA to YMPC-3001. DATA will be in the order of HIGH, MIDDLE, LOW BYTE .

※ Only for the first term of data transmission of a new title, 4 blocks of528bytes DECODING DATA will be transmitted and after then normally 3 blocks of 528byts will be sent to YMPC-3001 until next title comes.



DECODING TERMINATION FLOW

When DATA transmission is terminated(when HTRQ# is LOW), the Host controller will send a STOP COMMAND to YMPC-3001 as ADD=CVR, DATA=COMVEC_STOP.



DIGITAL EQ Function

Selecting DIGITAL EQ function

When YMPC-3001is in STOP or DECODING mode , DIGITAL EQ can be selected.
DIGITAL EQ band can be changed while YMPC-3001 is in the STOP or DECODING mode.
DIGITAL BASS will not operate when DIGITAL EQ is selected.
When Ready is in LOW status,the selected DIGITAL EQ COMMAND will be sent to YMPC-3001 as ADD=CVR,DATA=COMVEC_EQ_xxx(xxx=JAZ, CLA, POP, ROC, TEC).
DIGITAL EQ will be turned off when YMPC-3001is RESET.

DIGITAL EQ OFF

Host controller can turn the DIGITAL EQ OFF when YMPC-3001 is in STOP or DECODING processing.
When HTRQ# is LOW ,Host can send a DIGITAL EQ OFF COMMAND to YMPC-3001 as ADD=CVR,DATA=COMVEC_EQ_OFF.

DIGITAL BASS Function

Selecting DIGITAL BASS

When YMPC-3001is in STOP or DECODING mode , DIGITAL BASS can be selected.
DIGITAL EQ will not operate when DIGITAL BASS is selected.
When Ready is in LOW status,the selected DIGITAL BASS COMMAND will be sent to YMPC-3001 as ADD=CVR,DATA=COMVEC_DIG_BASS.
DIGITAL BASS will be turned off when YMPC-3001 is RESET .

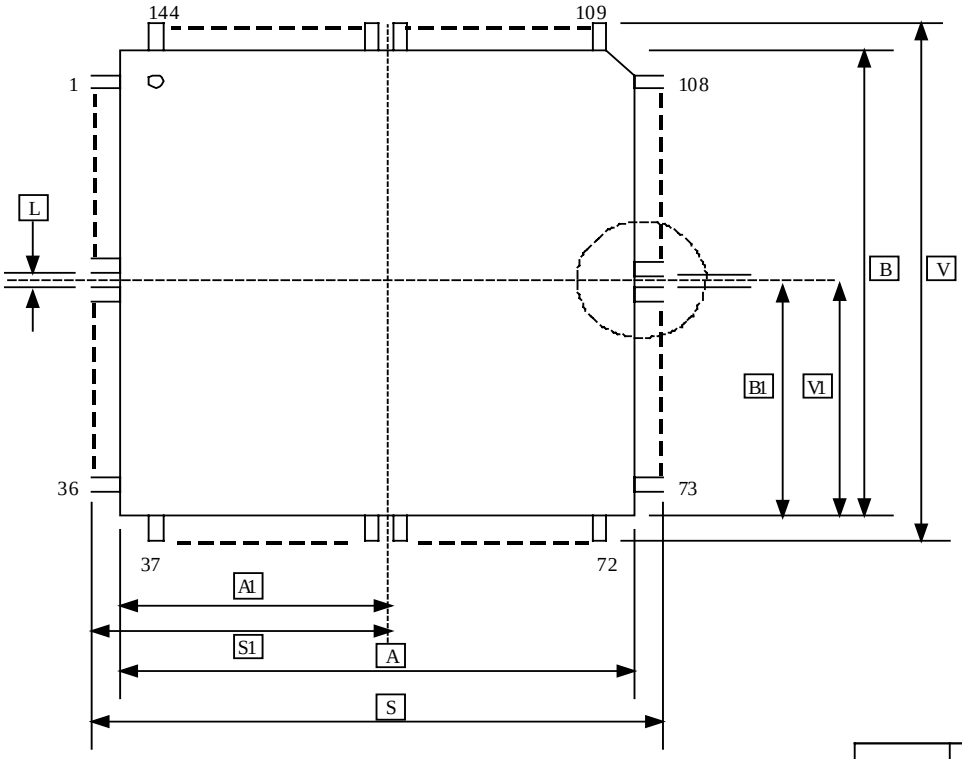
DIGITAL BASS OFF

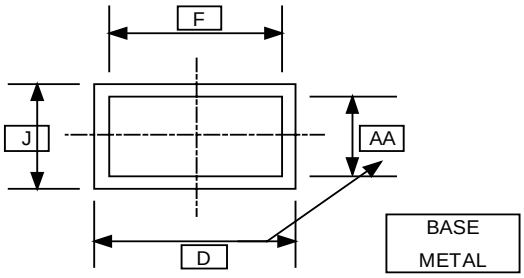
Host controller can turn the DIGITAL BASS OFF when YMPC-3001 is in STOP or DECODING processing.
When HTRQ# is LOW ,Host can send a DIGITAL BASS OFF COMMAND to YMPC-3001 as ADD=CVR,DATA=COMVEC_DIG_OFF.

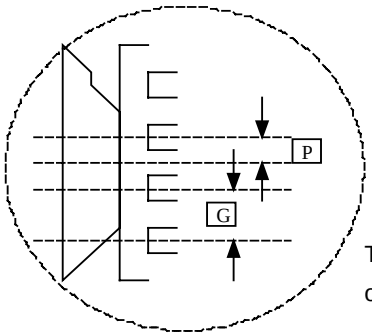
6.Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Input high voltage ¡¤ D(0:23), BG#, BB#, TA#, DE#, and PINIT/NMI# ¡¤ MOD[1]/IRQ[1], RESET, and TCK/TDI/TMS/ TRST/ESAI/Timer/HDI08/ SHI(SPI mode) pins ¡¤ SHI (I2C mode) pins ¡¤ EXTAL[8]	 Vin Vihp Vinx	 2.0 2.0 1.5 0.8 x Vcc	 - - -	 Vcc Vcc + 3.95 Vcc + 3.95 Vcc	 V
Input low voltage ¡¤ D(0:23), BG#, BB#, TA#, DE#, and PINIT/NMI# ¡¤ MOD[1]/IRQ[1], RESET, and TCK/TDI/TMS/ TRST/ESAI/Timer/HDI08/ SHI(SPI mode) pins ¡¤ SHI (I[2]C mode) pins ¡¤ EXTAL[8]	 Vin Vihp Vinx	 -0.3 -0.3 -0.3 -0.3	 - - -	 0.8 0,8 0.3 x Vcc 0.2 x Vcc	 V
Input leakage current	Iin	-10	-	10	mA
High impedance (off-state) input current(@ 2.4 V / 0.4 V)	Itsi	-10	-	10	mA
Output high voltage ¡¤ TTL (Ioh = -0.4 mA)[5,7] ¡¤ CMOS (Ioh = -10 mA)[5]	 Voh	 2.4 Vcc-0.01	 - -	 0.4 0.01	 V
Output low voltage ¡¤ TTL (Iol = 3.0 mA, open-drain pins Iol = 6.7 mA) ¡¤ CMOS (Iol = 10 mA)[5]	Vol	-	-	0.4 0.01	V
Input supply current[2] : (Operating frequency 100MHz for current measurements) ¡¤ In Normal mode decoding ¡¤ In Normal mode encoding ¡¤ In Wait mode ¡¤ In Stop mode[4]	 Icci Icci Iccw Iccs	 - - - -	 85 45 7.5 100	 - - 11 150	 mA mA mA uA
PLL supply current		-	1	2.5	mA
Input capacitance[5]	Cin	-	-	10	pF

7.Package Information





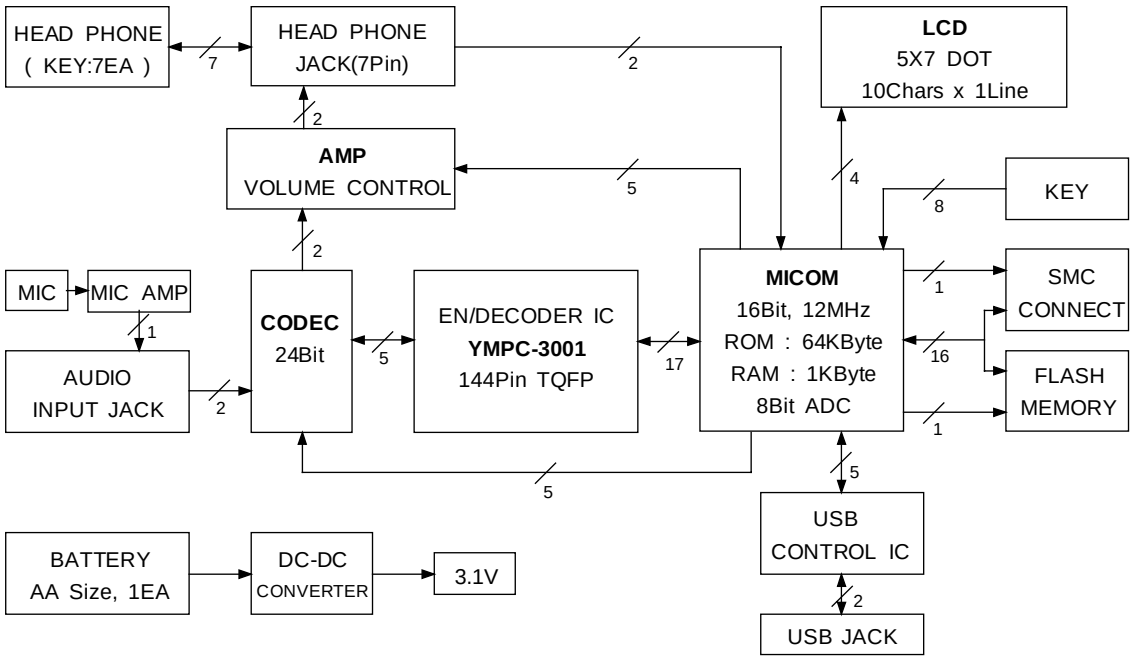


The Detailed View of the dotted circle area

DIM	MILLIMETERS	
	MIN	MAX
A	20.00BSC	
A1	10.00BSC	
B	20.00BSC	
B1	10.00BSC	
D	0.17	0.27
F	0.17	0.23
G	0.50BSC	
J	0.09	0.20
P	0.25BSC	
S	22.00BSC	
S1	11.00BSC	
V	22.00BSC	
V1	11.00BSC	
AA	0.09	0.16

8. Application Note(AN-2001)

-How to make a MP3 encoder/decoder system using YMPC-3001 .



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