WCT0006
6-Port Fast Ethernet Switch Controller

Rev. 00

DCN:WCT-300-SP-002

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1. Key Features

- High performance, stand alone, six-port 100/10Mbps fast Ethernet single-chip switch controller
- Target for cost/performance sensitive 6-port, 5-port, and 4-port switch or hub-switch application with the first two ports can be independently and individually programmable to be RMII or MII mode, half or full duplex mode, and speed/link mode
- Fastest latency time (7.2 us) for both unicast and broadcast
- Best broadcast throughput performance
- Best Novell-Performance3 client server performance
- Patent-pending per port output queueing architecture
- Support RMII/MII interface to PHY transceiver
- Provide packet switching functions between six on-chip100/10Mbps fast Ethernet ports
- Support both half & full duplex mode for all six ports
- Support 100/10Mbps auto-negotiation mode for all six ports
- Provide MDC/MDIO interface
- Incorporate six 802.3 compliant 100/10Mbps Media Access Controllers
- Built-in Address Translation Engine for self-learning and aging source addresses
- Support up to 2K unicast addresses and unlimited multicast/broadcast addresses
- Provide broadcast storm filtering
- Perform store and forward switching function and filtering at full wire speed
- Shared memory architecture with 32 bit data bus interface to Synchronous SRAM
- Intelligent network data buffer management for fairness among all six ports
- High visibility LED interface for displaying buffer utilization at each port
- Programmable VLAN mode enable receive packet size up to 1522 bytes
- Support back-pressure half duplex flow control
- Support IEEE 802.3x full duplex flow control
- Low-power 3.3v CMOS process
- 208 pin PQFP package

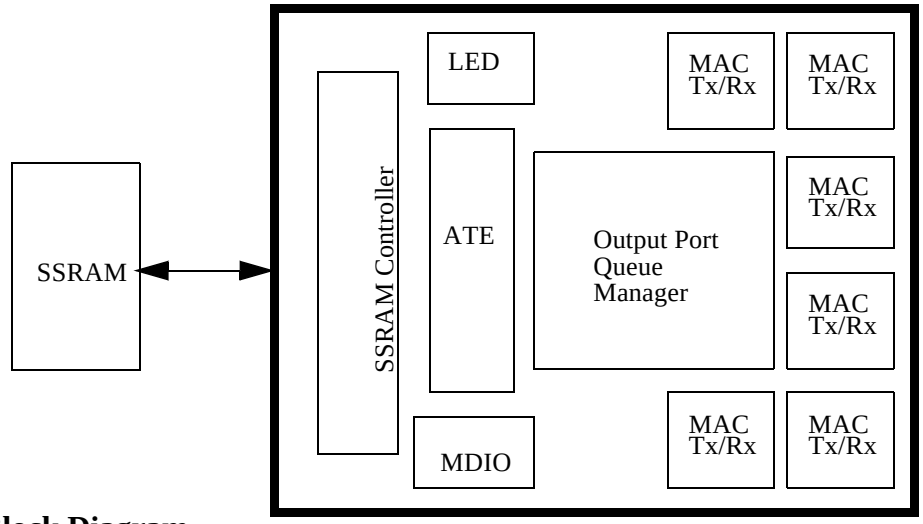

Figure 1. Main Block Diagram

2. Introduction

WCT0006 is an 6-Port 100/10 Mbps fast Ethernet switch/hub controller. It is a high performance and low cost single-chip solution for six-port fast Ethernet workgroup switch design. No CPU interface is required. It is a plug and play, self-running fast Ethernet switch controller. Figure 2. shows system block diagram of a complete 6-Port workgroup fast Ethernet switch.

WCT0006 supports 100/10Mbps auto-negotiation mode for all six ports. It provides MDC/MDIO management interface and supports RMII/MII interface for connecting external PHY transceiver. WCT0006 incorporates six IEEE 802.3x compliant 100/10Mbps MACs that support IEEE 802.3x full duplex and half duplex back pressure flow control. Its build-in Address Translation Engine provides support for self-learning and aging source addresses at full wire speed. WCT0006 advances the non-blocking output port architecture to allow both unicast and multicast packet enqueue/ dequeue at full wire speed. WCT0006 also features a viewing-capable LED interface for displaying buffer utilization at each port.

Further more, the Port 1 and Port 2 are individually programmable to be in fixed speed or auto-negotiation mode, in RMII or MII interface, in half_duplex or full_duplex mode, in Link or No Link mode.

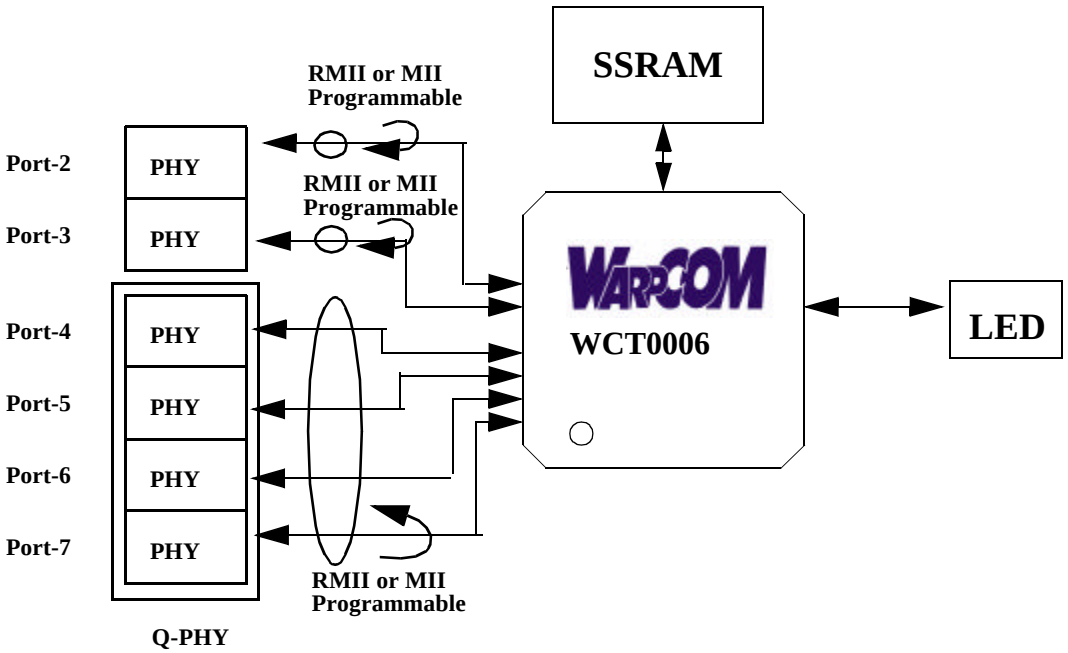

Figure 2. Complete 6-Port Workgroup Fast Ethernet Switch

3. Functional Blocks Overview

WCT0006 consists of the following major functional blocks: Fast Ethernet Port Interface, MDIO/MDC Management Interface, Address Translation Engine, SSRAM Interface, Output Port Queue Manager, and LED interface.

3.1 Fast Ethernet Port Interface

WCT0006 incorporates six IEEE 802.3 compliant 100/10Mbps fast Ethernet Media Access Control (MAC) ports. Reduced Media Independent Interface/Media Independent Interface (RMII/MII) is provided for glueless connection to off-the-shelf PHY chips. Each of the MAC supports both full duplex flow control and half duplex back pressure flow control. The full duplex flow control mode follows IEEE 802.3x standard. The half duplex flow control uses "force collision" at the receiving port when there is no buffer available for the incoming packet.

3.2 MDIO/MDC Management Interface

MDIO/MDC Management Interface is shared between 6 fast Ethernet ports. WCT0006 supports full auto-negotiation mode for capable PHYs. WCT0006 will continue to read PHYs registers through MDIO interface to find out the link status, duplex mode, speed, and the full duplex flow control during auto-negotiation mode.

3.3 Address Translation Engine (ATE)

ATE block does all address searching, address learning, and address aging. All functions are automatically enforced and all in default mode. Each entry in the external memory is 64 bits. 4Kx32 bits memory space from the external SSRAM is reserved for ATE memory. The default aging time is 420 seconds or 7 minutes. Within this time range, ATE block reads each entry in the 4Kx32 bits memory block and updates address table if necessary.

3.4 SSRAM Interface

WCT0006 directly interfaces to a 64Kx32 bits Synchronous SRAM. The SSRAM is used to store incoming and outgoing packets as well as the address table. The interface to SSRAM is glueless; all signals required to control SSRAM devices are provided. The SSRAM runs at 66MHz that provides enough bandwidth for all 6 ports to run at full duplex speed.

3.5 Output Port Queue Manager

WCT0006 features advanced built-in non-blocking output port queue architecture. The queue manager manages both enqueue of the incoming packets and dequeue of the outgoing packets at full wire speed. Each output port has its own queue. All input packets from input ports share a free buffer pool.

3.6 LED Interface

WCT0006 provides the view-capability of the LED interface for buffer utilization at each port. Two output pins are used for the LED serial interface. It can connect directly to the external 74164 latch devices for displaying the port status.

4.1 Logic Symbol Diagram (MII Interface)

Figure 3. Logic Symbol Diagram (MII Interface)

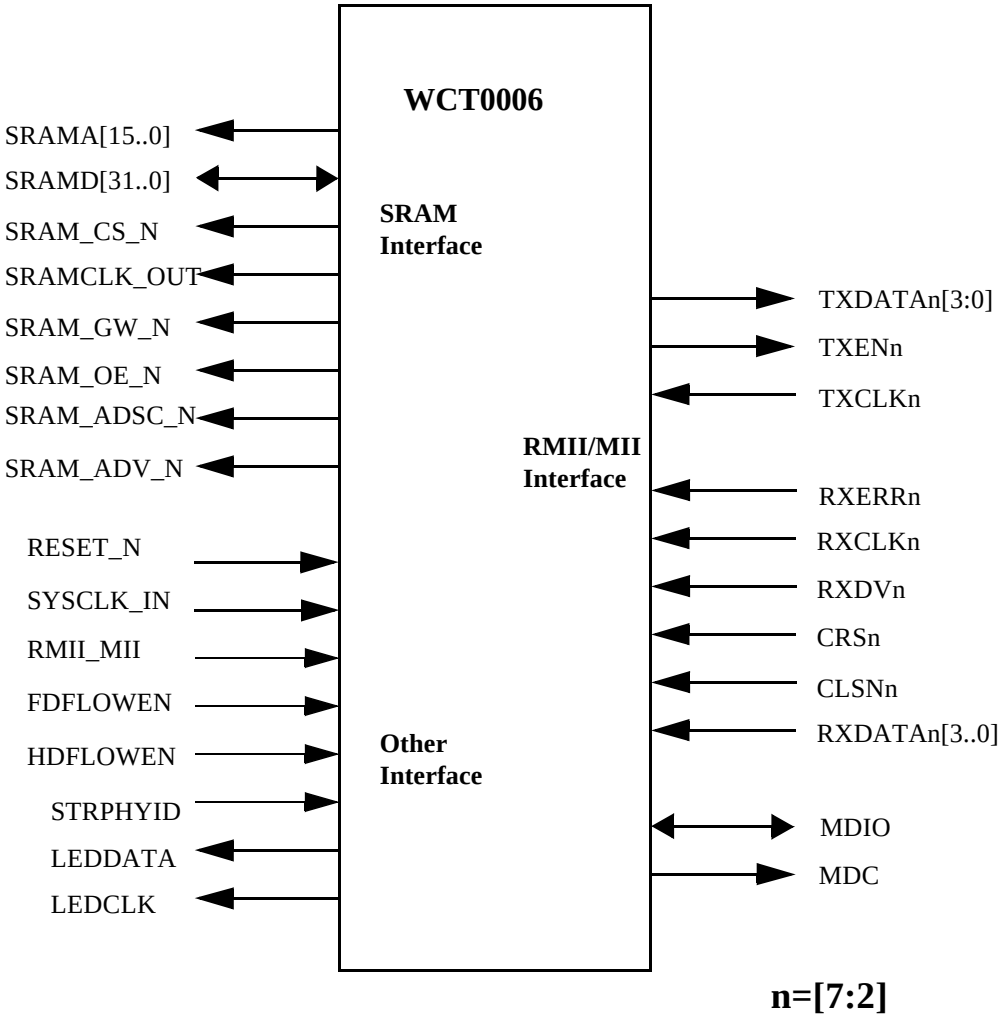

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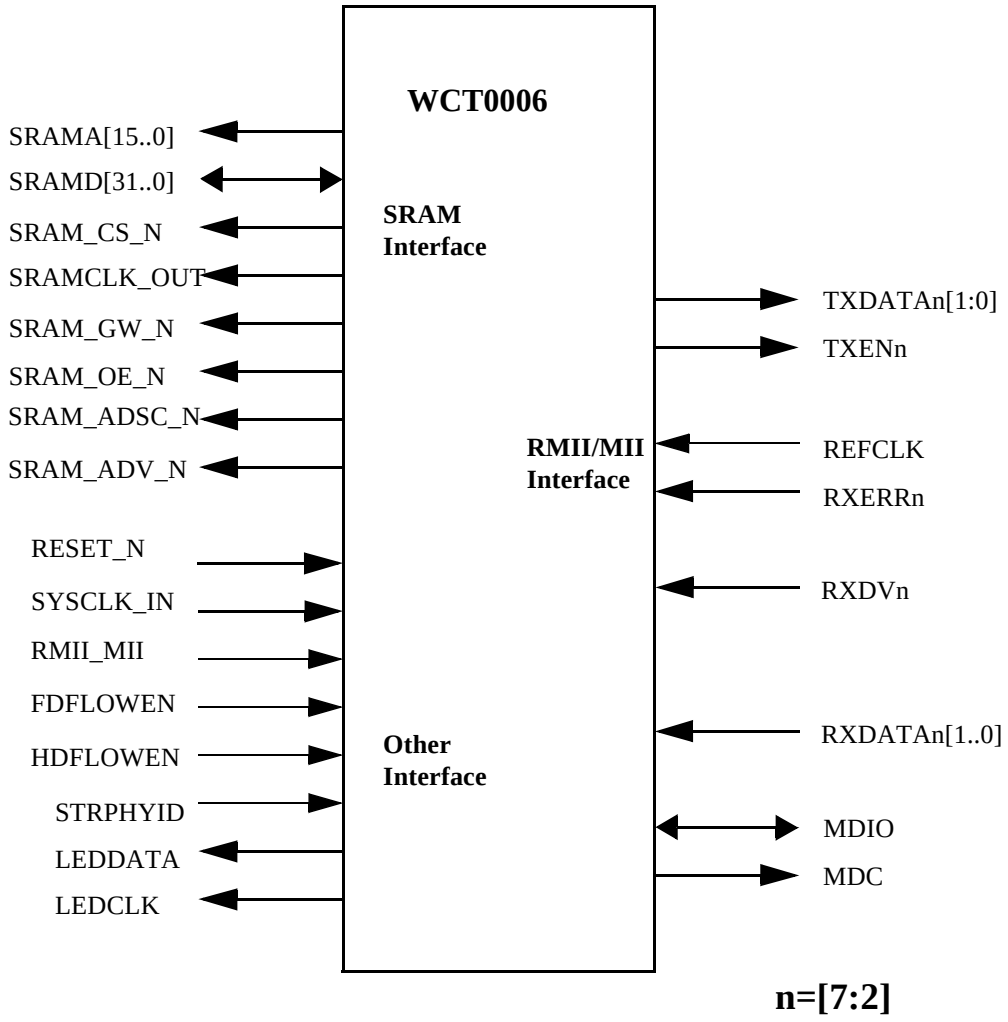
Figure 3. Logic Symbol Diagram (RMII Interface)



5. Functional Blocks Description

5.1 Fast Ethernet Port Interface

WCT0006 interfaces to 6 RMII/MII ports that are compliant with IEEE 802.3 standard. The RMII/MII interface allows WCT0006 to directly interface to any physical device with the same RMII/MII interface. WCT0006 incorporates all required digital circuitry to support different type of media: 100BaseTX, 100BaseT4, and 100BaseFX. Each of the RMII/MII ports has the following characteristics:

- Supports both 100Mbps and 10Mbps data rates in half or full duplex mode
- Supports both full duplex and half duplex back pressure flow control
- Provides 4 bit wide transmit and receive paths
- Uses TTL signal levels
- Provides simple management interface for auto-negotiation mode (common for all ports)

Media Access Control (MAC)

WCT0006 MAC performs all the functions in the 802.3 protocol such as frame formatting, frame stripping, CRC checking, deferral to link traffic, collision handling, and so on. The MAC receive block checks incoming packets and drops the bad packets including CRC error, alignment error, short packet (less than 64 bytes), and long packet (more than 1518 bytes or larger than 1522 bytes when VLAN mode is on). The transmit data append the 56 preamble bits and the 8 bits of Start Frame Delimiter (SFD) before the basic frame. The MAC transmit block constantly monitors the line. Actual transmission of the data onto network occurs only if it has been idle for a 96 bit period, a minimum interpacket gap (IPG) time. For the half duplex mode, it will also detect collision signal. If a collision is detected, the MAC transmits a JAM pattern and then delays the re-transmission for a random time period determined by the backoff algorithm. For full duplex mode, collision signal is ignored.

100/10 RMII/MII Compatible Interface

WCT0006 MAC can be connected to a 10Mbps or 100Mbps Ethernet network. Each MAC interfaces to an IEEE 802.3u 100/10 Mbps RMII/MII compatible physical device. WCT0006 can switch between 100 or 10 Mbps operation depending on speed of the network. The MAC clock inputs are driven by the physical device that controls clock rate based on auto-negotiation mode. In 100Mbps operation, both receive and transmit data are clocked at 25MHz. In 10Mbps operation, both receive and transmit data are clocked at 2.5MHz. The data path is 4 bits for both transmit and receive data.

Backoff

In half duplex mode, WCT0006 MAC implements the truncated exponential backoff algorithm defined in IEEE 802.3 standard. The MAC resets the collision counter after 16 consecutive re-transmit trials, then restarts the backoff algorithm and continues to retry and re-transmit the frame. A packet which continuously collides with a re-transmit signal will continue to be re-transmitted forever. However, the backoff intervals will change between the re-transmits. During a backoff period, there will be no data sending from WCT0006 and the TXEN signal at the RMII/MII interface is also disabled.

Half Duplex Flow Control

The back pressure flow control is used to throttle the end station to avoid dropping packets during network congestion situation. When the half duplex flow control pin HDFLOWEN is set, it enables back pressure half duplex flow control. WCT0006 uses "forced collision" scheme to perform half duplex flow control. When input free buffer is almost full, it will force a collision in the input port when WCT0006 senses an incoming packet. If the half duplex flow control mode is not set and there is no free buffer available for the incoming packet, the incoming packet will be dropped.

Full Duplex Flow Control

In full duplex mode, WCT0006 MAC supports the standard flow control defined in IEEE 802.3 Standard. It enables stopping of remote node transmissions. The basic mechanism for performing full duplex flow control is via a PAUSE operation.

The format of the PAUSE operation is as follows: Destination Address (6 bytes, 01-80-C2-00-00-01), Source Address (6 bytes), Type (2 bytes, 88-08), Op-Code (2 bytes, 00-01), Pause Time (2 bytes), Padding (42 bytes), FCS (4 bytes).

When the full duplex flow control pin FDFLOWEN is set in the configuration mode during reset, it enables full duplex flow control of WCT0006. In full duplex flow control, when input free buffer is almost empty or the output port buffer is almost full, WCT0006 will send out a PAUSE packet with pause time equal to "FFFF" to stop the remote node from sending more packets to output port. When the free buffer is available again, WCT0006 will send out a PAUSE packet with pause time equal to zero, indicating that the remote node may resume transmission. WCT0006 will also respond to the PAUSE command in the MAC receiving block. When the PAUSE command is detected, it will respond within one slot time to stop transmission of data frame for a specific amount of time defined in the pause time field of the PAUSE command packet.

RMII/MII Interface

WCT0006 supports two standard interfaces for each port. Each WCT0006 MAC contains a MII Interface for a MII compliant PHY device, and a RMII interface for a RMII compliant PHY device. Selection of RMII and MII Interface is controlled through the RMII_MII option input pin.

5.2 Management Interface

Each WCT0006 MAC contains a management interface for a MII/RMII compliant PHY device. This allows control and status parameters to be passed between WCT0006 and the PHY by one serial pin (MDIO) and a clocking pin (MDC). It also allows reducing the number of control pins required for PHY mode control.

SMI Cycles

The SMI protocol consists of a bit stream that is driven or sampled by the WCT0006 on each rising edge of the MDC clock. The bit stream format of the SMI frame is described in the following table. The MDC clock is running at 2.06MHz. (66/32= 2.06MHz)

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	D.D(16)	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	D.D(16)	Z

- PRE (Preamble). At the beginning of each transaction, WCT0006 sends a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.
- ST (Start of Frame). A Start of Frame pattern of 01.
- OP (Operation Code). 10 - Read; 01 - Write
- PHYAD (PHY Address). A 5 bit address of the PHY device (32 possible addresses). The first PHY address bit transmitted by WCT0006 is the MSB of the address.
- REGAD (Register Address). A 5 bit address of the PHY register (32 possible registers in each PHY). The first register address bit transmitted by WCT0006 is the MSB of the address. The WCT0006 always queries the PHY device for status of the link by reading register 1, bit 2.
- TA (Turn Around). The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of the SMI frame to avoid contention during a read transaction. During a Read transaction the PHY should not drive MDIO at the first bit time and drive "0" at the second bit time.
- DATA (Data). The data field is 16 bits long. The PHY drives the data field during Read transactions. WCT0006 drives the data field during write transactions. The first data bit transmitted and received shall be bit 15 of the PHY register being addressed.
- IDLE (Idle). The IDLE condition on MDIO is a high impedance state. The MDIO driver is disabled and the PHY should pull-up the MDIO line to a logic one.

Auto-Negotiation Mode

During auto-negotiation mode, WCT0006 continuously queries the PHY devices for their link status and the flow mode and the full duplex flow control capable status. The MAC link status and the flow mode of the chip will be updated accordingly. The predefined PHY addresses for link query are 10 to 15 (if STRPHYID pin is set to high) or 2 to 7 (if STRPHYID pin is set to low). The procedure for determining flow control mode are as follows:

1. Read the PHY control register 0, If bit 12 "auto-negotiation enable bit" is "0", it will just continue to read register 1 for link status and will not read register 4 and register 5. The speed is determined by the bit 13 of register 0: if reg0.13 is "1" => 100Mbps, if reg0.13 is "0" => 10Mbps. The duplex mode is determined by the bit 8: if reg0.8 is "1" => Full Duplex mode, if reg0.8 is "0" => Half Duplex mode.

   If register bit 12 is "1", auto-negotiation mode enabled, bit 0.13 & 0.8 will be overrided by register 4 & 5; it will read register 4 and 5 to decide the speed and duplex mode.
2. Read the PHY auto-negotiation complete status from PHY register 1, bit 5. As long as it is "0", it will switch to Half Duplex mode and continue to read PHY register bit 1.5. If it is "1", which means the auto-negotiation process is completed, it will continue to do step 3 up to step 7. The PHY bit 1.2 (Link Status) is read and latched during this same register read operation, regardless of the Auto-Negotiation status.
3. Read the Auto-Negotiation Advertisement register, PHY Register 4. Continue to step 4.
4. Read the Auto-Negotiation Link Partner Ability register, PHY Register 5. Continue to step 5.
5. Resolve the highest common ability of the two link partners in the following manner:
6. if (bit 4.8 AND bit 5.8) == "1" then ability is 100BASE-TX Full Duplex
7. else if (bit 4.9 AND bit 5.9) == "1" then ability is 100BASE-T4 Half Duplex
8. else if (bit 4.7 AND bit 5.7) == "1" then ability is 100BASE-TX Half Duplex
9. else if (bit 4.6 AND bit 5.6) == "1" then ability is 10BASE-T Full Duplex
10. else ability is 10BASE-T Half Duplex; Continue to step 6.
11. Resolve the duplex mode of the two link partners in the following manner:
12. if ((ability == "100BASE-TX Full Duplex") or (ability == "10BASE-T Full Duplex")) then duplex mode = FULL DUPLEX else duplex mode = HALF DUPLEX;
13. NOTE: the value of the duplex mode indication should change only after reading both PHY registers 4 and 5. Continue to step 7.
14. Update WCT0006 MAC. Go to step 1 again.

WCT0006 auto-negotiation mode also detects the pause operation enable bit for full duplex flow control. If the PHY register 4 bit 10 and register 5 bit 10 are both "1", the pause operation full duplex flow control will be enabled; otherwise, the pause operation full duplex flow control will not be enabled.

5.3 Address Translation Engine (ATE)

WCT0006 Address Translation Engine (ATE) block performs all address searching, address learning and address aging. Each entry in the external memory is 64 bit. The address table is organized as of 4kx32 bits and resides in the external SSRAM. The default aging time is 420 seconds or 7 minutes. Within this time frame, ATE block reads each entry of the 4kx32 memory block and updates them if necessary.

Address Searching

The address searching engine is used to search output port of the MAC destination address. It arbitrates the 6 input destination address and grants one lookup at a time. Two double words (64 bits) are read from SSRAM table, and status of the entry is compared with the entry's contents. If the compare matches, it returns the output port number to output port queue manager. The packet will be queued to the matched output port. If the compare does not match, the packet will be treated as a broadcast packet and will be sent to output ports. If the destination address is multicast address, the packet will be forwarded to all output ports.

Address Learning

The address learning engine is used to learn the source address. The address table is located in the external SSRAM. Up to 2k MAC address are stored in the address table. When the source address from an input packet can not be found in the address table, the ATE will enter into the self-learning mode and learn the source address. The new address will be added to the address table automatically.

Address Aging

The address aging process is used to ensure that if a node is disconnected from its segment and if its entry is removed from the address table.WCT0006 will run the address aging process continuously. The default aging time is 420 seconds or 7 minutes. Within this time frame, ATE block reads each entry of the 4kx32 memory block and updates the aging status bit.

Address Table: The address table in the SSRAM is as follows:

Bit Name	Offset	Size	Description
MAC Address	47:0	48	IEEE format MAC address
Valid	48	1	1: valid; 0: invalid
Age	49	1	1: aged; 0: not aged
Output port	63:56	8	output port number

5.4 Memory Interface

WCT0006 interfaces directly to the standard 2Mega bit (64Kx32) Synchronous SRAM (SSRAM). The SSRAM is running at 66MHz and the data bus is 32 bits. It can provide up to 2.1G bandwidth for data access. This memory bandwidth is enough for all 6 ports running at full wire speed in full duplex mode. The SSRAM is used to store incoming and outgoing packets as well as the address table. Memory buffer is partitioned into 2K bytes so that it can store up to the maximum Ethernet packet size (1518 bytes or 1522 bytes at VLAN mode). Memory controller provides the separate address and data bus as well as the control signals to the SSRAM. Burst data is initiated with the ADSC_N (Advanced Status Cache Controller) signal and the subsequent burst data is controlled by the ADV_N (Burst Address Advance) signal.

5.5 Queue Manager

WCT0006's queue manager uses an advanced non-blocking output port queue architecture. As a result, the output port queue architecture will not have the head-of-line blocking problem that is often encountered in the input port queue architecture.

The output port queues are controlled by an output port queue manager. This output port queue manager manages the enqueue of incoming packets and also the dequeue of outgoing packets at wire speed. When the packets coming from all input ports, queue manager ensures the free buffer was fairly granted to each of the input request. The input packet buffer is shared with all incoming packets from all input ports. Input packet buffer is managed by the free buffer queue link list that is also built in the chip to keep tracking the free buffer. In the case of multicast or broadcast packets, these packets are managed by the multicast queue manager. The multicast queue manager keeps tracking multicast packets to ensure the packets being sent to the proper output port. There are total of 6 output port queues maintained in WCT0006.

5.6 LED Interface

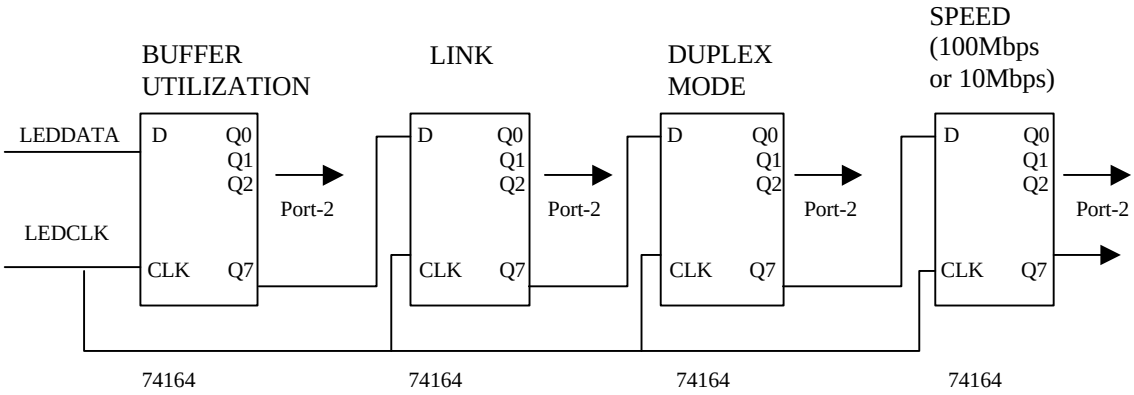
WCT0006 provides a simple LED interface which allows another option of utilizing port-status signals, in addition to utilizing signals from the PHY output. The choice is determined by PHY LED output functions, board layout design and total bill of material for the LED interface. The use of this LED interface in WCT0006 will ease board layout design since the design is independent of PHY LED functions. For detail design guidelines please refer to our application note.

Detail Design Guidelines for LED Interface in RMII Mode

- Use external 74164 as shift register for up to 24 status output.
- Two interface pins, LEDDATA and LEDCLK, are directly connect to the 74164.
- LEDCLK runs in120ns period for 32 cycles and keeps in high state for 20ms.
- Each port can have up to 4 statuses that are Link/Act, Duplex mode, Speed, and Buffer Utilization.
- Use one 74164 to display per port buffer status.
- Use two 74164 to display per port buffer status and LINK with RX flash.
- Use three 74164 to display per port buffer status, LINK with RX flash, and full/half duplex mode with Collision flash.

- Use four 74164 to display per port buffer status, LINK with RX flash, full/half duplex mode with Collision flash, and 100Mbps/10Mbps speed with TX flash.

DESIGN DIAGRAM FOR LED INTERFACE (RMII INTERFACE)



Port 2 to Port 7	Port 2 to Port 7	Port 2 to Port 7	Port 2 to Port 7
Output Port Buffer Status	LINK and RX/TX Status	Full or Half Duplex	100Mbps or 10Mbps
Full: "ON"	LINK: "ON"	Full_Duplex: "ON"	100Mbps: "ON"
Empty: "OFF"	No LINK: "OFF"	Half_Duplex: "OFF"	10Mbps: "OFF"
1% ~ 99%: "FLASH"	RX: "FLASH"	Collision: "FLASH"	TX: "FLASH"

For MII mode, the above sequence of 74164s will be LINK, DUPLEX MODE, SPEED 100/10, and BUFFER UTILIZATION.

6.1 Pin Diagram (MII Interface)

6.2 Pin Diagram (RMII Interface)

7.1 Pin Description (MII Interface)

Pin Name	Pin Number	Type	Description
Ethernet Access Port 2-7			
TXDATA2[3:0] TXDATA3[3:0] TXDATA4[3:0] TXDATA5[3:0] TXDATA6[3:0] TXDATA7[3:0]	40,41,42,43 57,58,59,60 74,75,76,77 91,92,93,94 109,110,111,112 126,127,128,129	O	Port 2-7 transmit data bit[3..0]: Outputs Port 2-7 Transmit Data. TXDATAn is synchronous to TXCLKn. In RMII interface, all TXDATAn[2:3] are not used and connected.
TXEN2 TXEN3 TXEN4 TXEN5 TXEN6 TXEN7	44 61 78 96 113 130	O	Port 2-7 transmit enable: Active HIGH. This output indicates that the packet is being transmitted. TXENn is synchronous to TXCLKn.
TXCLK2 TXCLK3 TXCLK4 TXCLK5 TXCLK6 TXCLK7	45 62 79 97 114 131	I	Port 2-7 transmit clock: Provides timing reference for the transfer of TXEN, TXDATA signals. TXCLK frequency is same as the data rate (25 MHz for 100Mbps, 2.5 MHz for 10Mbps). TXCLK nominal frequency should match nominal frequency of RXCLK for the same port. In RMII interface, all TXCLKn must be tied to GND
PRMII_MII2 PRMII_MII3 RXERR2 RXERR3 RXERR4 RXERR5 RXERR6 RXERR7	12 30 47 64 81 99 116 133	I	Port 2-7 receive error signal: Active HIGH. Indicates that an error was detected in the received frame. This input is ignored when RXDV for the same port is inactive. PRMII_MII2=1 to program Port 2 in RMII mode; PRMII_MII2=0 to program Port 2 in MII mode. PRMII_MII3=1 to program Port 3 in RMII mode; PRMII_MII3=0 to program Port 3 in MII mode.
RXCLK2 RXCLK3 RXCLK4 RXCLK5 RXCLK6 RXCLK7	48 65 82 100 117 134	I	Port 2-7 receive clock: Provides timing reference for the transfer of RXDV,RXDATA,RXERR signals (per port). Operates at either 25MHz for 100Mbps or 2.5 MHz for 10Mbps. The nominal frequency of RXCLK (per port) should match the nominal frequency of that port's TXCLK. In RMII interface, Pin-82 RXCLK4 is renamed to REFCLK, and all other pins must be tied to GND.

Pin Name	Pin Number	Type	Description
FIXFH_ATN2 FIXFH_ATN3 RXDV2 RXDV3 RXDV4 RXDV5 RXDV6 RXDV7	14 32 49 66 83 101 118 135	I	Port 2-7 receive data valid signal: Active High. Indicates that valid data is present on RXDATA lines. Synchronous to RXCLK. FIXFH_ATN2=1 to set Port 2 in FIX HDX/LINK mode; FIXFH_ATN2=0 to set Port 2 in Auto-negotiation mode. FIXFH_ATN3=1 to set Port 3 in FIX HDX/LINK mode; FIXFH_ATN3=0 to set Port 3 in Auto-negotiation mode.
FIXLNK2 FIXLNK3 CRS2 CRS3 CRS4 CRS5 CRS6 CRS7	15 33 50 67 84 102 119 136	I	Port 2-7 carrier sense signal. Active High. FIXLNK2=1 set LINK for Port 2 when FIXFH_ATN2=1; FIXLNK2=0 set NO LINK for Port2 when FIXFH_ATN2=1. FIXLNK3=1 set LINK for Port 3 when FIXFH_ATN3=1; FIXLNK3=0 set NO LINK for Port3 when FIXFH_ATN3=1. In RMII interface, all CRSn must be tied to GND
FIXHD_FD2 FIXHD_FD3 CLSN2 CLSN3 CLSN4 CLSN5 CLSN6 CLSN7	16 34 51 68 85 103 120 137	I	Port 2-7 collision detected: Active HIGH. Indicates a collision has been detected on the wire. This input is ignored in full duplex mode. CLSN is not synchronous to any clock. FIXHD_FD2=1 set HD for Port 2 when FIXFH_ATN2=1; FIXHD_FD2=0 set FD for Port2 when FIXFH_ATN2=1. FIXHD_FD3=1 set HD for Port 3 when FIXFH_ATN3=1; FIXHD_FD3=0 set FD for Port3 when FIXFH_ATN3=1. In RMII interface, all CLSNn must be tied to GND
RXDATA2[0:3] RXDATA3[0:3] RXDATA4[0:3] RXDATA5[0:3] RXDATA6[0:3] RXDATA7[0:3]	52, 53, 54, 55 69, 70, 71, 72 86, 87, 88, 89 104,105,106,107 121,122,123,124 138,139,140,141	I	Port 2-7 receive data bit[3..0]: Port 2-7 receive Data. Synchronous to RXCLKn. In RMII interface, all RXDATAn[2:3] are not used and connected to GND.
MDIO	142	I/O	RMII/MII Management Data I/O: This bidirectional line is used to transfer control information and status between PHY and WCT0006. It conforms with IEEE Standard 802.3u. This signal may be connected to PHY devices of the six ports. When not in use, this pin must be connected to a pulldown resistor.
MDC	143	O	RMII/MII Management Data Clock: Provides timing reference for the transfer of MDIO signal. This output may be connected to PHY devices of the six ports.
Memory Buffer Inter-face			

Pin Name	Pin Number	Type	Description
RESET_N	145	I	Power on reset: Active LOW. RESET_N must be asserted for at least 10 clock cycles when in reset state. Following RESET_N deassertion, WCT0006 clears the internal registers.
SYSCLK_IN	146	I	System Clock - 66.67 MHz: Provides the timing for WCT0006 internal units.
SRAMD[0:31]	165,166,167,169, 170,172,173,174, 175,176,177,178, 179,181,182,183, 184,185,186,187, 188,190,191,192, 193,194,196,197, 198,199,200,201	I/O	SSRAM Data: 32-bit SSRAM data bus. These signals connect directly to data I/O pins of the SSRAM device.
SRAMA[0:15]	148,149,150,151, 152,153,154,155, 156,158,159,160, 161,162,163,164	O	SSRAM Address Bus: These signals connect directly to address pins of the SSRAM device.
SRAM_CS_N	202	O	SSRAM chip select (active low)
SRAMCLK_OUT	204	O	System Clock Output for SSRAM
SRAM_GW_N	205	O	SSRAM write enable (active low)
SRAM_OE_N	206	O	SSRAM output enable (active low)
SRAM_ADSC_N	207	O	SSRAM ADSC signal (active low)
SRAM_ADV_N	208	O	SSRAM ADV signal (active low)
LED Interface			
LEDDATA	2	O	LED Data: Carries the serial data bit stream which contains the LED indicators per port. The data is shifted out using the LED-CLK.
LEDCLK	3	O	LED Clock: This output is used to clock LEDDATA output.
Power Pins			
GND	4, 22, 56, 63, 90, 108, 147, 168,180,189,203	Ground	Ground
VDD	17, 39, 73, 80,95, 125,144,157,171, 195	Power	Power Supply
Others			
RMII_MII	132	I	Set RMII_MII mode for Port 4,5,6, and 7. 0=MII interface(default). 1=RMII interface.

Pin Name	Pin Number	Type	Description
FDFLOWEN	1	I	Full duplex flow control enable: 0=enable full duplex flow control (default). 1=disable full duplex flow control.
HDFLOWEN	29	I	Half duplex back pressure enable: 0=enable half duplex back pressure flow control(default). 1=disable back pressure flow control.
STRPHYID	115	I	PHY Address control: 0=PHY starting address from 2 TO 7 (default). 1=PHY starting address from 10 TO 15.
OPT1	11	I	OPT1: Enable receiving VLAN tag (4 bytes); 0=Pass up to 1518 bytes(default). 1=Pass up to 1522 bytes.
TESTM1 TESTM2	46 98	I	TEST mode; 0=Normal mode. 1=For chip internal test only.
Unused Pins			
unused	10,13,18, 19, 20, 21,28,31,35, 36, 37, 38	I	These unused pins should be connected to GND
Not Connect Pins			
NC	5, 6, 7, 8,9 23,24,25,26,27	O	These output pins are not used and are not connected.

7.2 Pin Description (RMII Interface)

Pin Name	Pin Number	Type	Description
Ethernet Access Port 2-7			
TXDATA2[1:0] TXDATA3[1:0] TXDATA4[1:0] TXDATA5[1:0] TXDATA6[1:0] TXDATA7[1:0]	42,43 59,60 76,77 93,94 111,112 128,129	O	Port 2-7 transmit data bit[1..0]: Outputs Port 2-7 Transmit Data. These signals are transited synchronous with the rising edge of TXEN2-7. When TXEN2-7 asserts, then in each period of TXEN2-7, WCT0006 drives the recovered and encoded data into TXDATA2-7[1:0] for transmission. While TXEN2-7 is de-asserted then the TXDATA2-7[1:0] will have no effect upon the Reduced MII connecting device.
TXEN2 TXEN3 TXEN4 TXEN5 TXEN6 TXEN7	44 61 78 96 113 130	O	Port 2-7 transmit enable: This output indicates that the MAC is presenting di-bits on TXDATA2-7[1:0] on the Reduced MII for transmission. TXEN2-7 shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the Reduced MII. TXEN is synchronous to REFCLK.

Pin Name	Pin Number	Type	Description
PRMII_MII2 PRMII_MII3 RXERR2 RXERR3 RXERR4 RXERR5 RXERR6 RXERR7	12 30 47 64 81 99 116 133	I	Port 2-7 receive error signal: Active HIGH. Indicates that an error was detected in the received frame. This input is ignored when RXDV for the same port is inactive. PRMII_MII2=1 to program Port 2 in RMII mode; PRMII_MII2=0 to program Port 2 in MII mode. PRMII_MII3=1 to program Port 3 in RMII mode; PRMII_MII3=0 to program Port 3 in MII mode.
REFCLK	82	I	50MHz Reduced MII clock reference input. Synchronous clock reference for receive, transmit, and control interface.
FIXFH_ATN2 FIXFH_ATN3 RXDV2 RXDV3 RXDV4 RXDV5 RXDV6 RXDV7	14 32 49 66 83 101 118 135	I	Port 2-7 carrier sense and receive data valid signal: RXDV2-7 shall be asserted by the PHY when the receive medium nonidle. RXDV2-7 also shows that the receiving data is presenting on the RXDATA2-7[1:0] from Reduced MII connecting device. RXDV2-7 connect to CRS_DV2-7 of PHY with RMII interface. FIXFH_ATN2=1 to set Port 2 in FIX HDX/LINK mode; FIXFH_ATN2=0 to set Port 2 in Auto-negotiation mode. FIXFH_ATN3=1 to set Port 3 in FIX HDX/LINK mode; FIXFH_ATN3=0 to set Port 3 in Auto-negotiation mode.
FIXLNK2 FIXLNK3	15 33	I	FIXLNK2=1 set LINK for Port 2 when FIXFH_ATN2=1; FIXLNK2=0 set NO LINK for Port2 when FIXFH_ATN2=1. FIXLNK3=1 set LINK for Port 3 when FIXFH_ATN3=1; FIXLNK3=0 set NO LINK for Port3 when FIXFH_ATN3=1.
FIXHD_FD2 FIXHD_FD3	16 34	I	FIXHD_FD2=1 set HD for Port 2 when FIXFH_ATN2=1; FIXHD_FD2=0 set FD for Port2 when FIXFH_ATN2=1. FIXHD_FD3=1 set HD for Port 3 when FIXFH_ATN3=1; FIXHD_FD3=0 set FD for Port3 when FIXFH_ATN3=1.
RXDATA2[0:1] RXDATA3[0:1] RXDATA4[0:1] RXDATA5[0:1] RXDATA6[0:1] RXDATA7[0:1]	52, 53 69, 70 86, 87 104,105 121,122 138,139	I	Port 2-7 receive data bit[1..0]: These bundle signals are input from the Reduced MII connecting device. RXD2-7[1:0] shall transition synchronously to REFCLK. For each clock period in which RXDV2-7 is asserted, RXD2-7[1:0] transfers two bits of recovered data from the PHY.
MDIO	142	I/O	RMII/MII Management Data I/O: This bidirectional line is used to transfer control information and status between PHY and WCT0006. It conforms with IEEE Standard 802.3u. This signal may be connected to PHY devices of the six ports. When not in use, this pin must be connected to a pulldown resistor.
MDC	143	O	RMII/MII Management Data Clock: Provides timing reference for the transfer of MDIO signal. This output may be connected to PHY devices of the six ports.
Memory Buffer Inter-face			

Pin Name	Pin Number	Type	Description
RESET_N	145	I	Power on reset: Active LOW. RESET_N must be asserted for at least 10 clock cycles when in reset state. Following RESET_N deassertion, WCT0006 clears the internal registers.
SYSCLK_IN	146	I	System Clock - 66.67 MHz: Provides the timing for WCT0006 internal units.
SRAMD[0:31]	165,166,167,169, 170,172,173,174, 175,176,177,178, 179,181,182,183, 184,185,186,187, 188,190,191,192, 193,194,196,197, 198,199,200,201	I/O	SSRAM Data: 32-bit SSRAM data bus. These signals connect directly to data I/O pins of the SSRAM device.
SRAMA[0:15]	148,149,150,151, 152,153,154,155, 156,158,159,160, 161,162,163,164	O	SSRAM Address Bus: These signals connect directly to address pins of the SSRAM device.
SRAM_CS_N	202	O	SSRAM chip select (active low)
SRAMCLK_OUT	204	O	System Clock Output for SSRAM
SRAM_GW_N	205	O	SSRAM write enable (active low)
SRAM_OE_N	206	O	SSRAM output enable (active low)
SRAM_ADSC_N	207	O	SSRAM ADSC signal (active low)
SRAM_ADV_N	208	O	SSRAM ADV signal (active low)
LED Interface			
LEDDATA	2	O	LED Data: Carries the serial data bit stream which contains the LED indicators per port. The data is shifted out using the LED-CLK.
LEDCLK	3	O	LED Clock: This output is used to clock LEDDATA output.
Power Pins			
GND	4, 22, 56, 63, 90, 108, 147, 168,180,189,203	Ground	Ground
VDD	17, 39, 73,80, 95, 125,144,157,171, 195	Power	Power Supply
Others			
RMII_MII	132	I	Set RMII_MII mode for Port 4,5,6, and 7. 0=MII interface(default). 1=RMII interface.

Pin Name	Pin Number	Type	Description
FDFLOWEN	1	I	Full duplex flow control enable: 0=enable full duplex flow control (default). 1=disable full duplex flow control.
HDFLOWEN	29	I	Half duplex back pressure enable: 0=enable half duplex back pressure flow control(default). 1=disable back pressure flow control.
STRPHYID	115	I	PHY Address control: 0=PHY starting address from 2 TO 7 (default). 1=PHY starting address from 10 TO 15.
OPT1	11	I	OPT1: Enable receiving VLAN tag (4 bytes); 0=Pass up to 1518 bytes(default). 1=Pass up to 1522 bytes.
TESTM1 TESTM2	46 98	I	TEST mode; 0=Normal mode. 1=For chip internal test only.
Unused Pins			
unused	10,13,18,19,20, 21,28,31,35,36, 37,38,45,48, 50,51,54,55,62, 65,67,68,71, 72,79,84,85, 88,89,97,100, 102,103,106,107, 114,117,119,120, 123,124,131,134, 136,137,140,141	I	These unused pins should be connected to GND
Not Connect Pins			
NC	5,6,7,8,9, 23,24,25,26,27 40,41,57,58,74, 75,91,92,109, 110,126,127	O	These output pins are not used and are not connected.

8.1 Pin Reference Table (MII Interface)

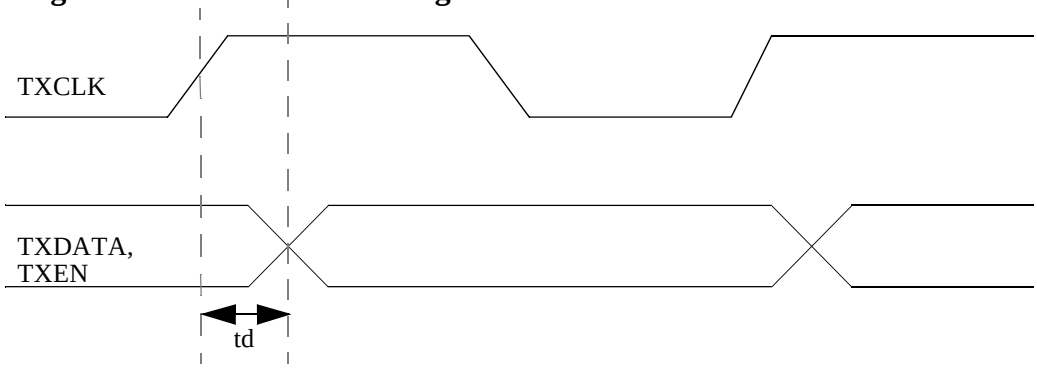
Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	FDFLOWEN	45	TXCLK2	89	RXDATA4[3]	133	RXERR7	177	SRAMD[10]
2	LEDDATA	46	TESTM1	90	GND	134	RXCLK7	178	SRAMD[11]
3	LEDCLK	47	RXERR2	91	TXDATA5[3]	135	RXDV7	179	SRAMD[12]
4	GND	48	RXCLK2	92	TXDATA5[2]	136	CRS7	180	GND
5	NC	49	RXDV2	93	TXDATA5[1]	137	CLSN7	181	SRAMD[13]
6	NC	50	CRS2	94	TXDATA5[0]	138	RXDATA7[0]	182	SRAMD[14]
7	NC	51	CLSN2	95	VDD	139	RXDATA7[1]	183	SRAMD[15]
8	NC	52	RXDATA2[0]	96	TXEN5	140	RXDATA7[2]	184	SRAMD[16]
9	NC	53	RXDATA2[1]	97	TXCLK5	141	RXDATA7[3]	185	SRAMD[17]
10	unused	54	RXDATA2[2]	98	TESTM2	142	MDIO	186	SRAMD[18]
11	OPT1	55	RXDATA2[3]	99	RXERR5	143	MDC	187	SRAMD[19]
12	PRMII_MII2	56	GND	100	RXCLK5	144	VDD	188	SRAMD[20]
13	unused	57	TXDATA3[3]	101	RXDV5	145	RESET_N	189	GND
14	FIXFH_ATN2	58	TXDATA3[2]	102	CRS5	146	SYSCLK_IN	190	SRAMD[21]
15	FIXLNK2	59	TXDATA3[1]	103	CLSN5	147	GND	191	SRAMD[22]
16	FIXHD_FD2	60	TXDATA3[0]	104	RXDATA5[0]	148	SRAMA[0]	192	SRAMD[23]
17	VDD	61	TXEN3	105	RXDATA5[1]	149	SRAMA[1]	193	SRAMD[24]
18	unused	62	TXCLK3	106	RXDATA5[2]	150	SRAMA[2]	194	SRAMD[25]
19	unused	63	GND	107	RXDATA5[3]	151	SRAMA[3]	195	VDD
20	unused	64	RXERR3	108	GND	152	SRAMA[4]	196	SRAMD[26]
21	unused	65	RXCLK3	109	TXDATA6[3]	153	SRAMA[5]	197	SRAMD[27]
22	GND	66	RXDV3	110	TXDATA6[2]	154	SRAMA[6]	198	SRAMD[28]
23	NC	67	CRS3	111	TXDATA6[1]	155	SRAMA[7]	199	SRAMD[29]
24	NC	68	CLSN3	112	TXDATA6[0]	156	SRAMA[8]	200	SRAMD[30]
25	NC	69	RXDATA3[0]	113	TXEN6	157	VDD	201	SRAMD[31]
26	NC	70	RXDATA3[1]	114	TXCLK6	158	SRAMA[9]	202	SRAM_CS_N
27	NC	71	RXDATA3[2]	115	STRPHYID	159	SRAMA[10]	203	GND
28	unused	72	RXDATA3[3]	116	RXERR6	160	SRAMA[11]	204	SRAMCLK_OUT
29	HDFLOWEN	73	VDD	117	RXCLK6	161	SRAMA[12]	205	SRAM_GW_N
30	PRMII_MII3	74	TXDATA4[3]	118	RXDV6	162	SRAMA[13]	206	SRAM_OE_N
31	unused	75	TXDATA4[2]	119	CRS6	163	SRAMA[14]	207	SRAM_ADSC_N
32	FIXFH_ATN3	76	TXDATA4[1]	120	CLSN6	164	SRAMA[15]	208	SRAM_ADV_N
33	FIXLNK3	77	TXDATA4[0]	121	RXDATA6[0]	165	SRAMD[0]		
34	FIXHD_FD3	78	TXEN4	122	RXDATA6[1]	166	SRAMD[1]		
35	unused	79	TXCLK4	123	RXDATA6[2]	167	SRAMD[2]		
36	unused	80	VDD	124	RXDATA6[3]	168	GND		
37	unused	81	RXERR4	125	VDD	169	SRAMD[3]		
38	unused	82	RXCLK4	126	TXDATA7[3]	170	SRAMD[4]		
39	VDD	83	RXDV4	127	TXDATA7[2]	171	VDD		
40	TXDATA2[3]	84	CRS4	128	TXDATA7[1]	172	SRAMD[5]		
41	TXDATA2[2]	85	CLSN4	129	TXDATA7[0]	173	SRAMD[6]		
42	TXDATA2[1]	86	RXDATA4[0]	130	TXEN7	174	SRAMD[7]		
43	TXDATA2[0]	87	RXDATA4[1]	131	TXCLK7	175	SRAMD[8]		
44	TXEN2	88	RXDATA4[2]	132	RMII_MII	176	SRAMD[9]		

8.2 Pin Reference Table (RMII Interface)

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	FDFLOWEN	45	unused	89	unused	133	RXERR7	177	SRAMD[10]
2	LEDDATA	46	TESTM1	90	GND	134	unused	178	SRAMD[11]
3	LEDCLK	47	RXERR2	91	NC	135	RXDV7	179	SRAMD[12]
4	GND	48	unused	92	NC	136	unused	180	GND
5	NC	49	RXDV2	93	TXDATA5[1]	137	unused	181	SRAMD[13]
6	NC	50	unused	94	TXDATA5[0]	138	RXDATA7[0]	182	SRAMD[14]
7	NC	51	unused	95	VDD	139	RXDATA7[1]	183	SRAMD[15]
8	NC	52	RXDATA2[0]	96	TXEN5	140	unused	184	SRAMD[16]
9	NC	53	RXDATA2[1]	97	unused	141	unused	185	SRAMD[17]
10	unused	54	unused	98	TESTM2	142	MDIO	186	SRAMD[18]
11	OPT1	55	unused	99	RXERR5	143	MDC	187	SRAMD[19]
12	PRMII_MII2	56	GND	100	unused	144	VDD	188	SRAMD[20]
13	unused	57	NC	101	RXDV5	145	RESET_N	189	GND
14	FIXFH_ATN2	58	NC	102	unused	146	SYSCLK_IN	190	SRAMD[21]
15	FIXLNK2	59	TXDATA3[1]	103	unused	147	GND	191	SRAMD[22]
16	FIXHD_FD2	60	TXDATA3[0]	104	RXDATA5[0]	148	SRAMA[0]	192	SRAMD[23]
17	VDD	61	TXEN3	105	RXDATA5[1]	149	SRAMA[1]	193	SRAMD[24]
18	unused	62	unused	106	unused	150	SRAMA[2]	194	SRAMD[25]
19	unused	63	GND	107	unused	151	SRAMA[3]	195	VDD
20	unused	64	RXERR3	108	GND	152	SRAMA[4]	196	SRAMD[26]
21	unused	65	unused	109	NC	153	SRAMA[5]	197	SRAMD[27]
22	GND	66	RXDV3	110	NC	154	SRAMA[6]	198	SRAMD[28]
23	NC	67	unused	111	TXDATA6[1]	155	SRAMA[7]	199	SRAMD[29]
24	NC	68	unused	112	TXDATA6[0]	156	SRAMA[8]	200	SRAMD[30]
25	NC	69	RXDATA3[0]	113	TXEN6	157	VDD	201	SRAMD[31]
26	NC	70	RXDATA3[1]	114	unused	158	SRAMA[9]	202	SRAM_CS_N
27	NC	71	unused	115	STRPHYID	159	SRAMA[10]	203	GND
28	unused	72	unused	116	RXERR6	160	SRAMA[11]	204	SRAMCLK_OUT
29	HDFLOWEN	73	VDD	117	unused	161	SRAMA[12]	205	SRAM_GW_N
30	PRMII_MII3	74	NC	118	RXDV6	162	SRAMA[13]	206	SRAM_OE_N
31	unused	75	NC	119	unused	163	SRAMA[14]	207	SRAM_ADSC_N
32	FIXFH_ATN3	76	TXDATA4[1]	120	unused	164	SRAMA[15]	208	SRAM_ADV_N
33	FIXLNK3	77	TXDATA4[0]	121	RXDATA6[0]	165	SRAMD[0]		
34	FIXHD_FD3	78	TXEN4	122	RXDATA6[1]	166	SRAMD[1]		
35	unused	79	unused	123	unused	167	SRAMD[2]		
36	unused	80	VDD	124	unused	168	GND		
37	unused	81	RXERR4	125	VDD	169	SRAMD[3]		
38	unused	82	REFCLK	126	NC	170	SRAMD[4]		
39	VDD	83	RXDV4	127	NC	171	VDD		
40	NC	84	unused	128	TXDATA7[1]	172	SRAMD[5]		
41	NC	85	unused	129	TXDATA7[0]	173	SRAMD[6]		
42	TXDATA2[1]	86	RXDATA4[0]	130	TXEN7	174	SRAMD[7]		
43	TXDATA2[0]	87	RXDATA4[1]	131	unused	175	SRAMD[8]		
44	TXEN2	88	unused	132	RMII_MII	176	SRAMD[9]		

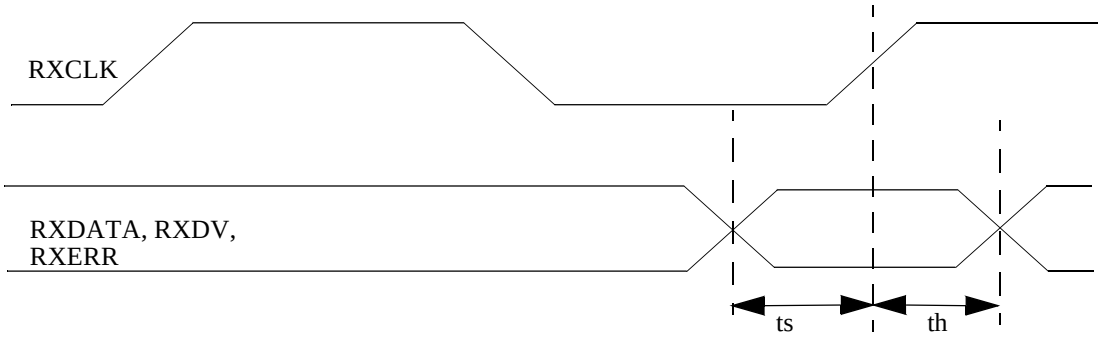
9. Timing Diagrams

Figure 5. MII Transmit Timing



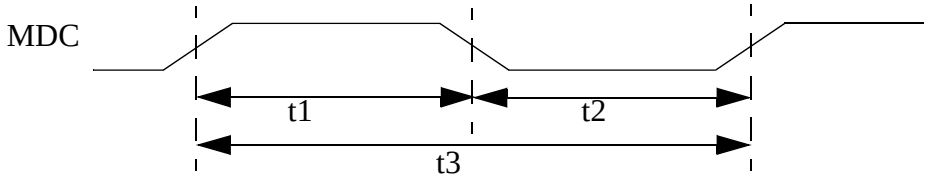
Name	Parameter	Min.	Max.	Units
td	Valid Delay after Rising TXCLK	2	15	ns

Figure 6. MII Receive Timing



Name	Parameter	Min.	Max.	Units
ts	Setup Time to Rising RXCLK	6		ns
th	Hold Time after Rising RXCLK	3		ns

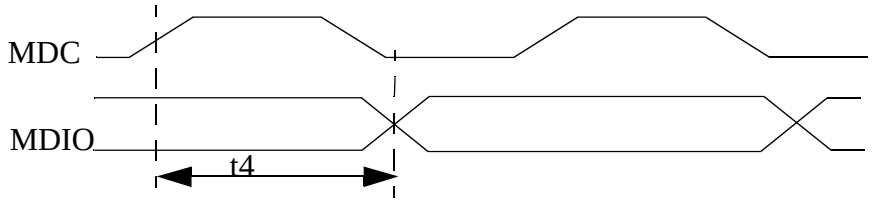
Figure 7. MDC Waveform



Name	Parameter	Typical	Units
t1	MDC High Time	240	ns
t2	MDC Low Time	240	ns
t3[1]	MDC Period	480	ns

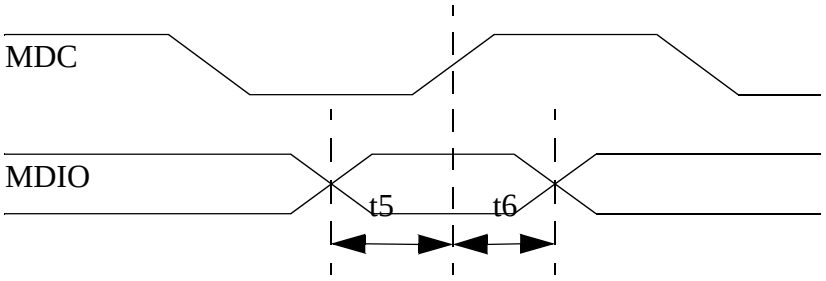
Note 1. MDC is generated internally by dividing the CLK clock input by 32. CLK clock frequency of 66MHz is assumed.

Figure 8. MDIO Output Delay



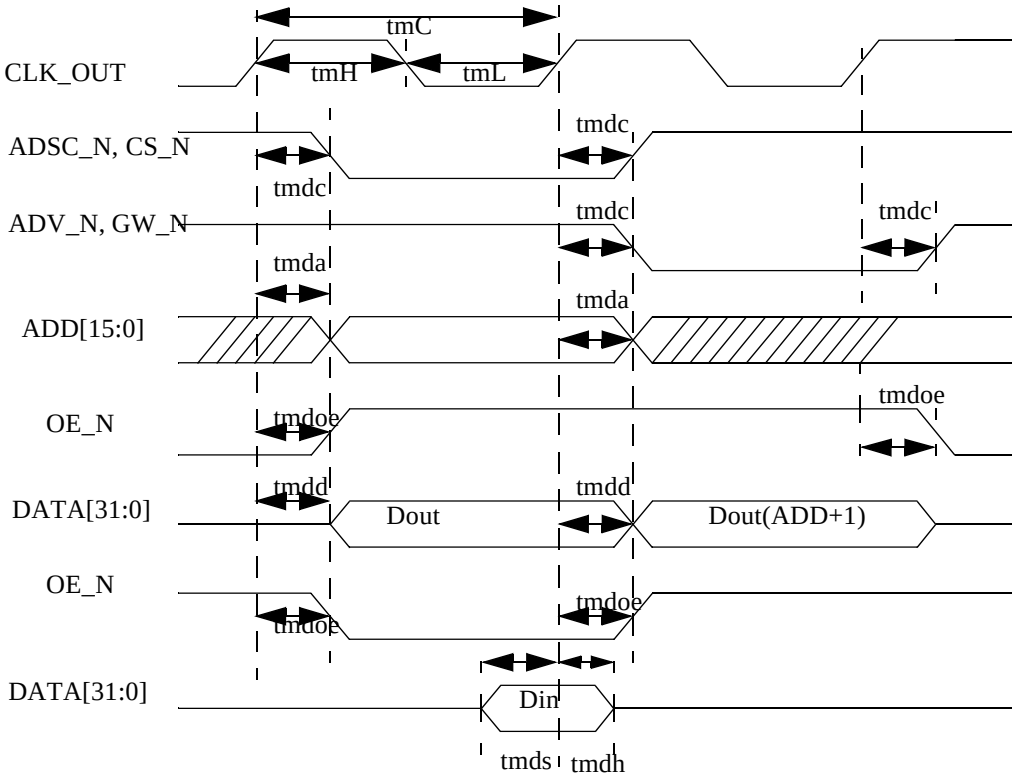
Name	Parameter	MIN.	MAX.	UNITS
t4	Rising MDC to Valid MDIO	10	250	ns

Figure 9. MDIO Setup and Hold Time



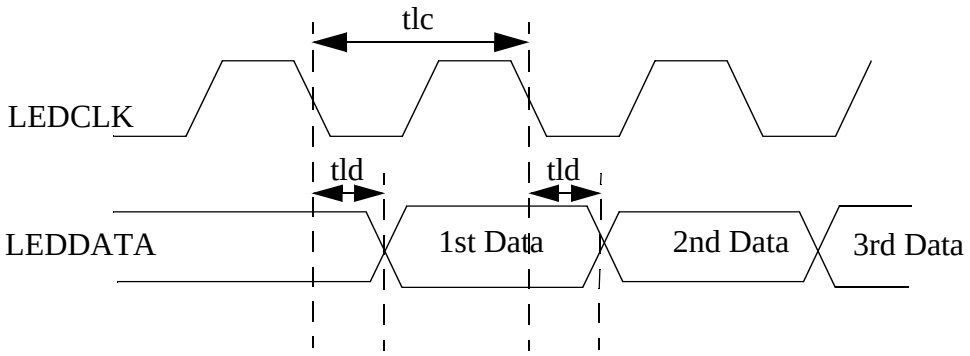
Name	Parameter	MIN.	MAX.	UNITS
t5	Setup time to Rising MDC	10		ns
t6	Hold Time after Rising MDC	10		ns

Figure 10. SSRAM Timing



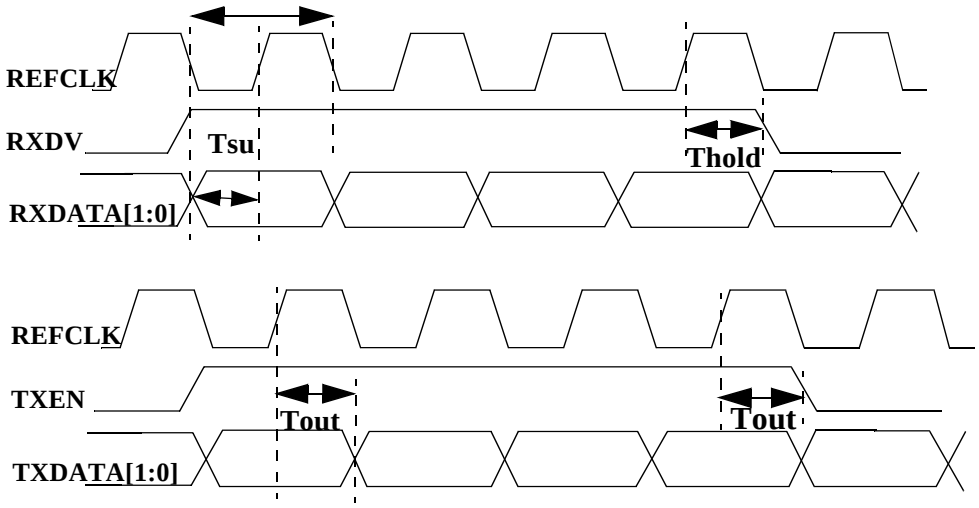
Name	Description	Min	Max	Units
tmC	SSRAM clock cycle time	15		ns
tmH	SSRAM clock high time	6		ns
tmL	SSRAM clock low time	6		ns
tmds	Data in setup time	5		ns
tmdh	Data in hold time	0		ns
tmdd	Data out delay	1	6	ns
tmda	Address out delay	1	6	ns
tmdoe	OE_N out delay	1	6	ns
tmdc	ADSC_N, ADV_N, CS_N, GW_N out delay	1	6	ns

Figure 11. LED Interface Timing



Name	Parameter	Min	Max	Units
tlc	LEDCLK period		150	ns
tld	Delay from LEDCLK falling to LEDDATA	0	20	ns

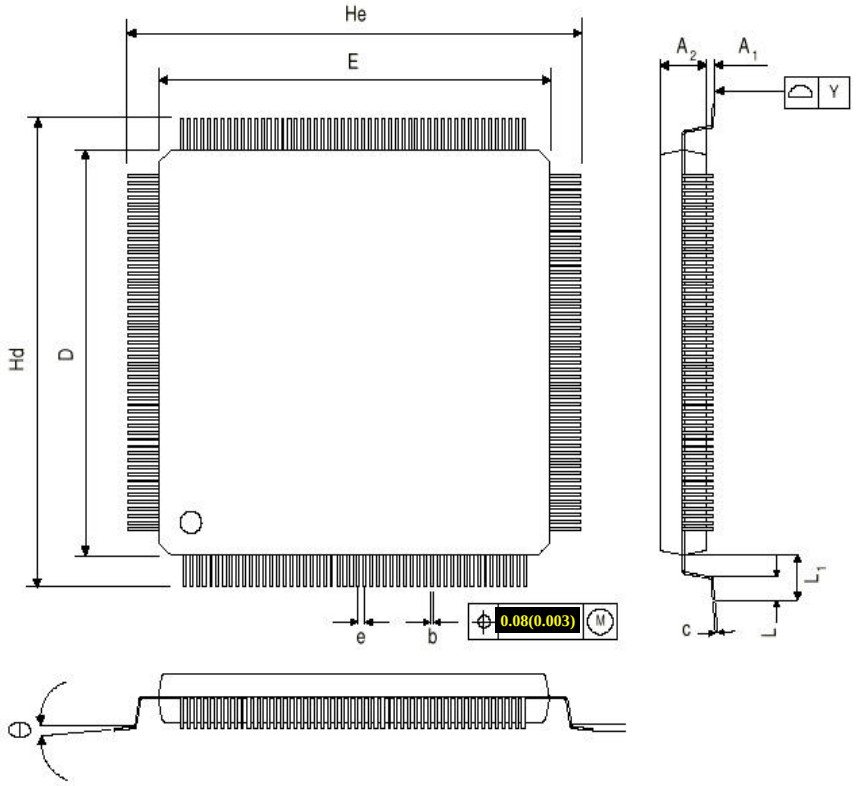
Figure 12. RMII Receive and Transmit Timing



Name	Parameter	Min	Max	Units
Tsu	Setup time for the RXDV, RXDATA to the REFCLK	2		ns
Thold	Hold time for the RXDV, RXDATA to the REFCLK	2		ns
Tout	Delay time for the TXEN, TXDATA to the REFCLK	2	10	ns

10. Package Diagram

FIGURE 12: 208 Lead PQFP Package Outline



208 PQFP PACKAGE DIMENTIONS (mm)

Symbol	Min.	Nom.	Max.
A_1	0.10		
A_2	3.10	3.23	3.35
b	0.17	0.20	0.23
c	0.10	0.15	0.25
D	27.67	28.00	28.13
E	27.67	28.00	28.13
e	0.45	0.50	0.55
Hd	30.30	30.60	30.90
He	30.30	30.60	30.90
L	0.30	0.50	0.70
L_1	1.10	1.30	1.50
Y			0.10
⏀	0^0		10^0

11. DC Characteristics

Recommended Operation Conditions

Symbol	Parameter	Min	Type	Max	Unit
V_{CC}	Power Supply	3.1	3.3	3.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		70	^{0}C
I_{CC}	V_{CC} Current			500mA	

DC Electrical Characteristics for 3.3 volts Operations

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 4, 8 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} =4, 8 mA	2.4		V

General DC Characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
I_I	Input Current		-10		10	uA
I_{OZ}	Tri-state Leakage Current		-10		10	uA
C_{IN}	Input Capacitance			5	10	PF
C_{OUT}	Output Capacitance			5	10	PF
C_{BID}	Bi-directional Buffer Capacitance			5	10	PF

Absolute Maximum Ratings

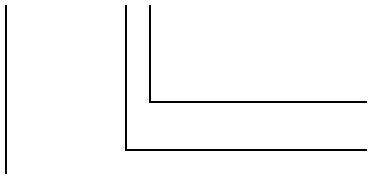
Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	^0C

Notes:

- Conditions beyond those listed for the absolute maximum will destroy or damage the products.
- Conditions for sustained periods at or near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage performance and/or function.

12. Order Information

WCT0006 PC



Chip Revision

Package Type P: Plastic Quad Flat Pack

Part Type: 6-Port Fast Ethernet Switch Controller

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San Jose, CA 95131
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Patent Pending No. 09/238,711; 09/239,210

WARPCOM DOCUMENT CONTROL RELEASE FORM

SUBJECT (1) **Data Sheet: WCT0006** **6-Port Fast Ethernet Switch Controller**	DOCUMENT CONTRL NO. 002 DOCUMENT NO. WCT-300-SP-002 REV. NO. 00 COMPLETE DATE 6/2/1999

CHANGE INFORMATION

CHANGE FROM: (*attached document if applicable*) [**X**] Original [**X**] Change	**CHANGE TO:** (*attached document if applicable*)
Rename the product from: WCT-E006	Rename the product to: WCT0006
Support only MII Interface	Support both RMII/MII Interface
	Separate Paragraph 7.1 Pin Description (MII Interface) from Paragraph 7.2 Pin Description (RMII Interface)
	In RMII interface, these un-used input pins are named as *unused* in Paragraph 6.2 Pin Diagram, Paragraph 7.2 Pin Description, and Paragraph 8.2 Pin Reference Table.
RXERR2-7 are wrongly described as ***unused*** and tied to GND in the following paragraphs: • Paragraph 4.2. Logic Symbol Diagram (RMII Interface) • Paragraph 6.2. Pin Diagram (RMII Interface) • Paragraph 7.1. Pin Description (MII Interface) • Paragraph 7.2. Pin Description (RMII Interface) and in ***unused*** pins • Paragraph 8.2 Pin Reference Table (RMII Interface)	RXERR2-7 are recovered and required as inputs in the following paragraphs: • Paragraph 4.2. Logic Symbol Diagram (RMII Interface) • Paragraph 6.2. Pin Diagram (RMII Interface) • Paragraph 7.1. Pin Description (MII Interface) • Paragraph 7.2. Pin Description (RMII Interface) and recovered from ***unused*** pins • Paragraph 8.2 Pin Reference Table (RMII Interface)
	Add TABLE OF CONTENTS and cover page

SPECIFY THE CHANGED PAGE NUMBERS IF APPLICABLE	Total: 33 Pages (not including this DCN Control page)

1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*
16	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*	*25*	*26*	*27*	*28*	*29*	*30*
31	*32*	*33*												