UE6005

Time-Code Receiver IC

1 Short Description

The UE6005 is a bipolar integrated straight through receiver circuit, which is suitable for the frequency range from 40kHz up to 120 kHz (ASK modulation).
The IC receives and demodulates time code signals transmitted by e.g. DCF77 (Germany), MSF (UK), WWVB (USA) and JJY (JPN).
The device is designed for radio controlled clock applications with very high sensitivity.
Integrated functions as stand by mode and complementary output stages offer features for universal applications.

2 Features

- Low power consumption
- Very high sensitivity (0.4µV)
- High selectivity by using crystal filter
- Power down mode available
- Only a few external components necessary
- Complementary output stages
- AGC hold mode
- Wide frequency range (40 ... 120 kHz)
- Low power battery applications (1.1 .. 3.6 V)

Block Diagram

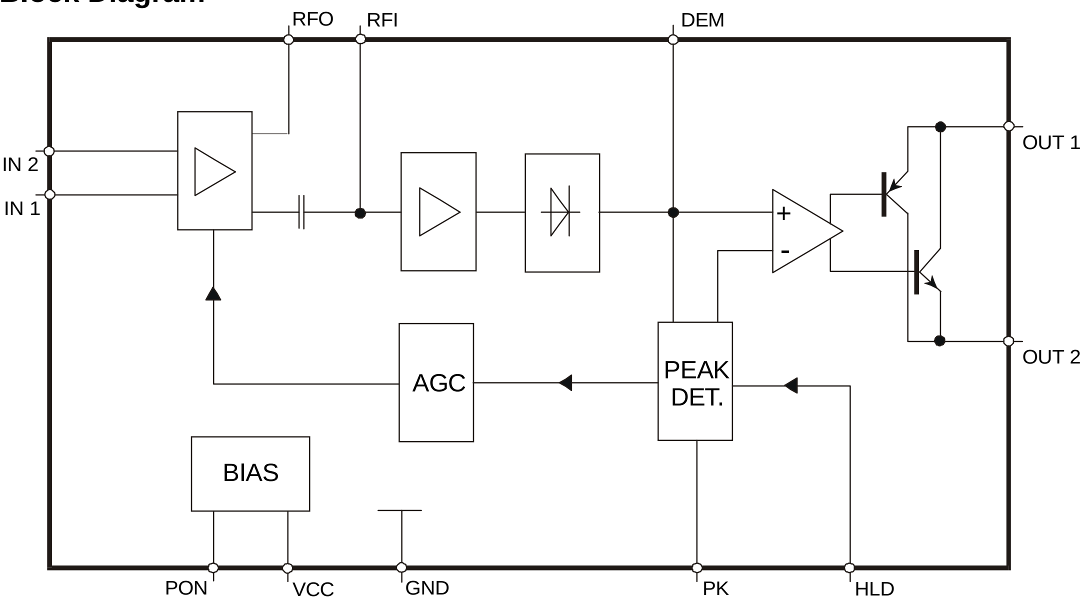


Figure 1. Block diagram

3 Ordering Information

Extended Type Number	Package	Remarks
UE6005 DIT	No	Die in trace
UE6005 FB	Yes	SSO16
UE6005 FBG3	Yes	SSO16, taped and reeled
UE6005 DBQ	No	CSP Chip Scale Package

4 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	VCC	5.5	V
Ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range	R_{stg}	-55 to +150	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883 D HBM)	$\pm V_{ESD}$	2000	V

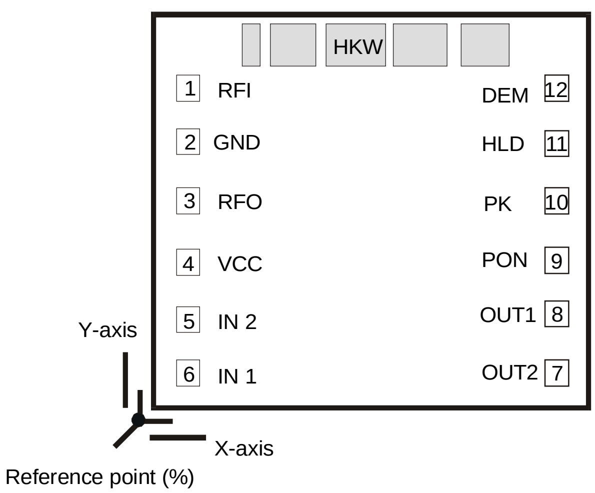
5 PAD Coordinates

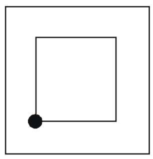
The UE6005 is available as die for "chip-on-board" mounting and in SSO16 package.
DIE size: 1.65 x 1.44 mm
PAD size: 100 x 100 µm (contact window 88 x 88 µm)
Thickness: 300 µm ± 10 µm

Symbol	Function	x-axis (µm)	y-axis (µm)	Pad # (dice)	Pin # (SSO16*)
RFI	RF-input (from crystal)	130	1141	1	2
GND	Ground	130	934	2	3
RFO	RF-output (to crystal)	130	727	3	4
VCC	Supply voltage	130	520	4	5
IN 2	Antenna input 2	130	313	5	6
IN 1	Antenna input 1	130	106	6	7
OUT 2	Negative signal output	1430	106	7	10
OUT 1	Positive signal output	1430	313	8	11
PON	Power on input	1430	520	9	12
PK	Peak detector output	1430	727	10	13
HLD	AGC hold	1430	934	11	14
DEM	Demodulator output	1430	1141	12	15

*Pin 1,8,9 and 16 not connected

6 Pad Layout





The PAD coordinates are referred to the left bottom point of the contact window

NOTE:
If conductive glue is used for DIE-placement then the DIE-pad has to be connected to GND.

Figure 2. Pad layout

Pin Layout SSO16

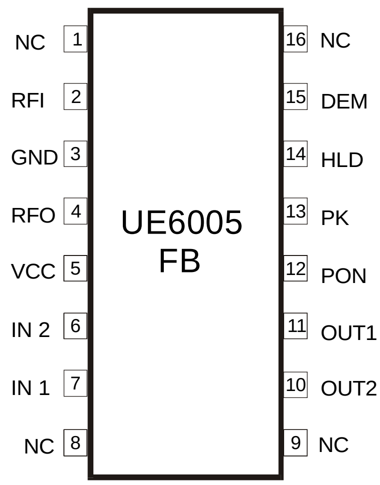


Figure 3. Pin layout SSO16

IN 1, IN 2

A ferrite antenna is connected between IN 1 and IN 2. For high sensitivity, the Q factor of the antenna circuit should be as high as possible. Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. We recommend a Q factor between 40 and 150, depending on the application. An optimal signal-to-noise ratio will be achieved by a resonator resistance of 40 kΩ to 100 kΩ.

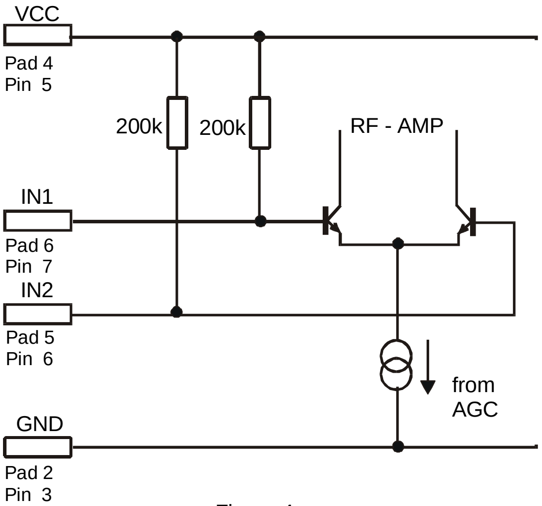


Figure 4.

RFO

In order to achieve a high selectivity, a crystal is connected between the Pins RFO and RFI. It is used with the serial resonant frequency according to the time-code transmitter (e.g., 60 kHz WWVB, 60 kHz MSF, 77.5 kHz DCF or 40 kHz JJY) and acts as a serial resonator. The given parallel capacitor of the filter crystal (about 0.8 pF) is internally compensated so that the bandwidth of the filter is about 10 Hz. The impedance of RFI is high. Parasitic loads have to be avoided.

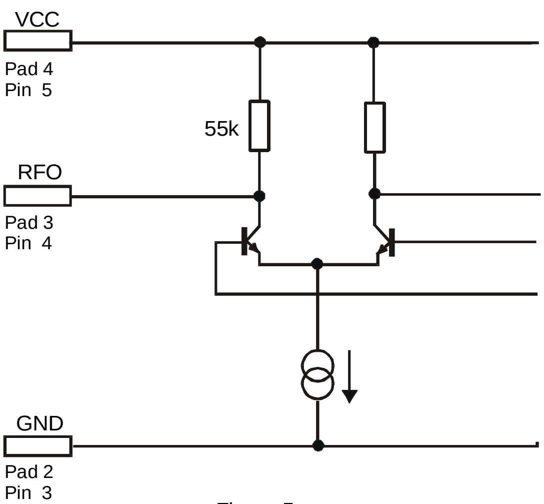


Figure 5.

RFI

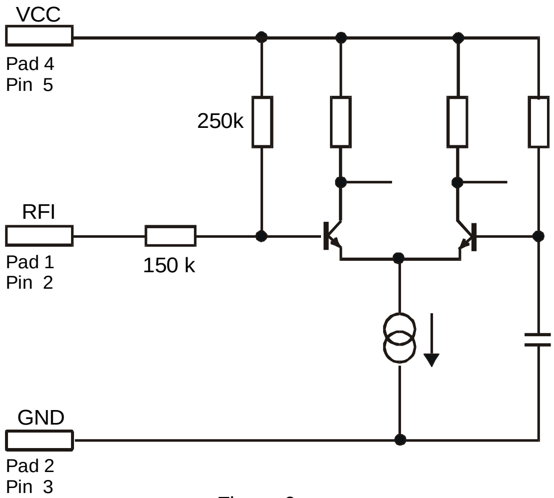


Figure 6.

DEM

Demodulator output. To ensure the function, an external capacitor has to be connected at this output.

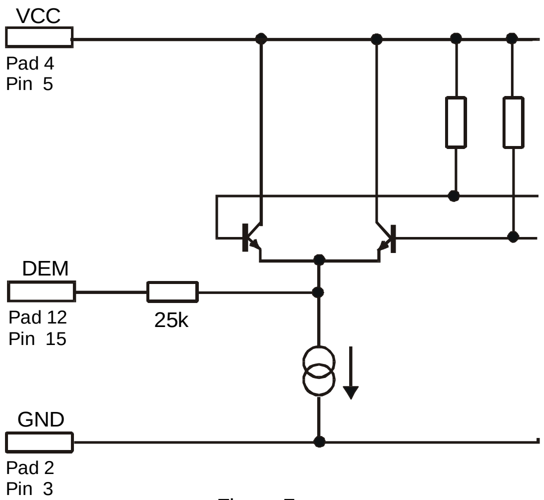


Figure 7.

HLD

AGC hold mode: HLD high (V_{HLD} = V_{CC}) sets normal function, HLD low (V_{HLD} = 0) holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor.

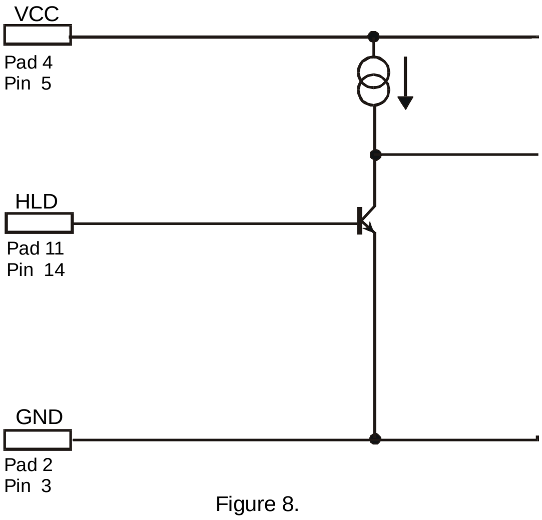


Figure 8.

PK

Peak detector output: An external capacitor has to be connected to ensure the function of the peak detector. The value of the capacitance influences the AGC regulation time.

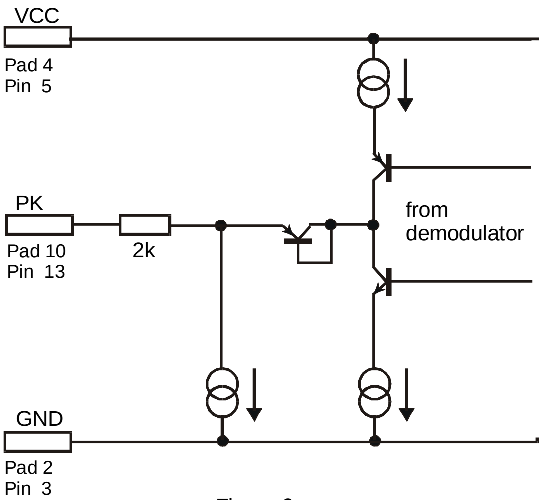


Figure 9.

VCC, GND

V_{CC} and GND are the supply voltage inputs. To power down the circuitry it is recommended to use the PON input and not to switch the power supply. Switching the power supply effects in a long power up waiting time.

PON

If PON is connected to GND, the receiver will be activated. The set-up time is typically 0.5 s after applying GND at this pin. If PON is connected to V_{CC}, the receiver will switch to power-down mode.

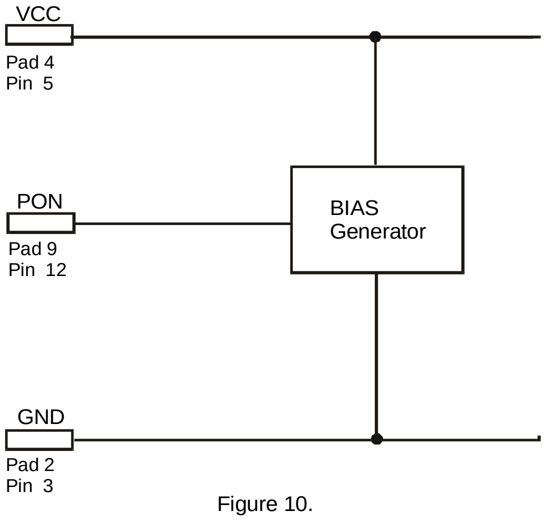


Figure 10.

OUT 1, OUT 2

The serial signal of the time-code transmitter can be directly decoded by a micro controller. Details about the time-code format of several transmitters are described separately.
The output consists of a combination of a NPN / PNP open collector stage. The function depends on the external circuitry:

- A load resistor is connected from OUT1 to V_{CC}, OUT2 is connected to GND. This performs the functionality of a NPN open collector stage.
- A load resistor is connected from OUT2 to GND, OUT1 is connected to V_{CC}. This performs the functionality of a PNP open collector stage.

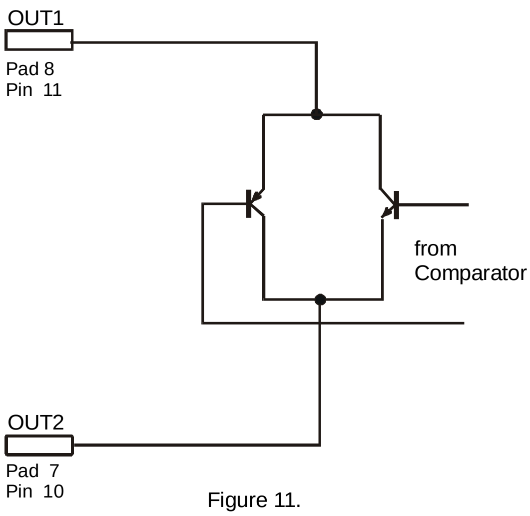


Figure 11.

7 Design Hints

7.1 Dimensioning of antenna circuit for different clock/watch applications

The bar antenna is a very critical device of the complete clock receiver. Observing some basic RF design rules helps to avoid possible problems. The IC requires a resonant resistance of 40 kΩ to 100 kΩ. This can be achieved by a variation of the L/C-relation in the antenna circuit.
To get a resonant resistance inside of this required range we recommend to use antenna capacitors of a value between 2.2nF and 6.8nF. The optimum value of capacitor has to be specified respecting the concrete application and different marginal conditions (type of ferrite material, type of antenna wire, available space for antenna-bobbin etc.).
It is not easy to measure such high resistances in the RF region. A more convenient way is to distinguish between the different bandwidths of the antenna circuit and to calculate the resonant resistance afterwards.
Thus, the first step in designing the antenna circuit is to measure the bandwidth. Figure 12 shows an example for the test circuit. The RF signal is coupled into the bar antenna by inductive means, e.g., a wire loop. It can be measured by a simple oscilloscope using the 10:1 probe. The input capacitance of the probe, typically about 10 pF, should be taken into consideration. By varying the frequency of the signal generator, the resonant frequency can be determined.

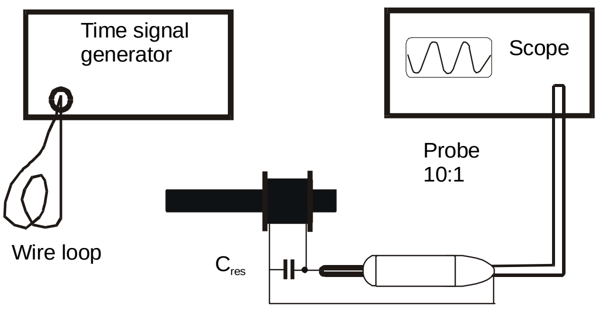


Figure 12.

At the point where the voltage of the RF signal at the probe drops by 3 dB, the two frequencies can then be measured. The difference between these two frequencies is called the bandwidth BW_A of the antenna circuit. As the value of the capacitor C_{res} in the antenna circuit is known, it is easy to compute the resonant resistance according to the following formula:

$$R_{res} = \frac{1}{2 \times \pi \times BW_A \times C_{res}}$$

Where
R_{res} is the resonant resistance,
BW_A is the measured bandwidth
C_{res} is the value of the capacitor in the antenna circuit (Farad).

If high inductance values and low capacitor values are used, the additional parasitic capacitance of the coil must be considered. The Q value of the capacitor should be no problem if a high Q type is used. The Q value of the coil differs more or less from the DC resistance of the wire. Skin effects can be observed but do not dominate.

Therefore, it should not be a problem to achieve the recommended values of the resonant resistance. The use of thicker wire increases the Q value and accordingly reduces bandwidth. This is advantageous in order to improve reception in noisy areas. On the other hand temperature compensation of the resonant frequency might become a problem if the bandwidth of the antenna circuit is low compared to the temperature variation of the resonant frequency. Of course, the Q value can also be reduced by a parallel resistor.

Temperature compensation of the resonant frequency is a must if the clock is used at different temperatures. Please ask your supplier of bar antenna material and of capacitors for specified values of the temperature coefficient.

Furthermore, some critical parasitics have to be considered. These are shortened loops (e.g., in the ground line of the PCB board) close to the antenna and undesired loops in the antenna circuit. Shortened loops decrease the Q value of the circuit. They have the same effect like conducting plates close to the antenna. To avoid undesired loops in the antenna circuit, it is recommended to mount the capacitor C_{res} as close as possible to the antenna coil or to use a twisted wire for the antenna-coil connection. This twisted line is also necessary to reduce feedback of noise from the microprocessor to the IC input. Long connection lines must be shielded.
A final adjustment of the time-code receiver can be carried out by pushing the coil along the bar antenna.

7.2 Dimensioning of external circuitry in correspondence to different time-signals

The value of 22nF for capacitor C_{DEM}, as specified in the test-circuitry shown in chapters 9) and 10), represents the minimum needed for a frequency of 77.5 kHz. For lower frequencies (40kHz, 60kHz) should be used at least a value of C_{DEM} = 47nF. For a better suppression of noise and other disturbances it is recommended to double the values of C_{DEM}. That means, C_{DEM} = 47nF for 77.5kHz and C_{DEM} = 100nF for 40kHz and 60kHz. This optimisation has to be done in function of the concrete application.

8 Electrical Characteristics

VCC = 3V, reference point Pin 3, input signal frequency 77.5 kHz ± 5 Hz; carrier voltage 100% reduction to 25% for t_{MOD} = 200ms; t_{amb} = 25°C, unless otherwise specified.

Parameter	Test condition / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pad/Pin V_{CC}	V_{CC}	1.1		3.6	V
Supply current	Pad/Pin V_{CC}	I_{CC}		200	250	µA
Set-up time after V_{CC} ON	V_{CC} = 3V	t		1.5		s
Reception frequency range		F_{in}	40		120	kHz
Minimum input voltage	Pad/Pin IN1, IN2 Rout ≥ 100kOhm	V_{in}		0.4	0.6	µV
Maximum input voltage	Pad/Pin IN1, IN2	V_{in}	30	50		mV
Input amplifier max. gain (V_{PK} = 0.1V)		V_{U1}		53		dB
Input amplifier min. gain (V_{PK} = 0.8V)		V_{U2}		-40		dB
Output voltage (OUT 1,low) External circuitry like npn Open collector stage	V_I = 100 µV; $I_{OUT1\,L}$ = 30 µA	$V_{OUT1\,L}$			0.3	V
Output voltage (OUT 2, high) External circuitry like pnp Open collector stage	V_I = 100 µV; $I_{OUT2\,H}$ = 30 µA	$V_{OUT2\,H}$	V_{cc}- 0.5	V_{cc} - 0.3		V
Output current (OUT 1 high) External circuitry like npn Open stage collector	V_I = 100 µV; 100% amplitude	$I_{OUT1\,H}$			1	µA
Output current (OUT 1 low) External circuitry like npn Open stage collector	V_I = 100 µV; 25% amplitude	$I_{OUT1\,L}$			500	µA
Output current (OUT 2, high) External circuitry like pnp Open collector stage	V_I = 100 µV; 25% amplitude	- $I_{OUT2\,H}$			500	µA
Output current (OUT 2, low) External circuitry like npn Open collector stage	V_I = 100 µV 100% amplitude	- $I_{OUT2\,L}$			1	µA

Power-ON control; PON Pad/Pin PON

Switch current receiver ON	V_{PON} = 0 V, Pad PON	- I_{PON}		14	20	µA
Quiescent current receiver OFF	V_{PON}=V_{CC}, Pad/Pin V_{CC}	I_{CC0}			0.5	µA
Set-up time after PON		t		0.5	2	s

AGC hold mode; HLD Pad/Pin HLD

Switch voltage receiver normal mode	V_{HLD} = V_{CC}	V_{HLD}	V_{CC} - 0.2			V
Input current AGC in hold mode	V_{HLD} = 0 V	-I_{HLD}			2	µA

AC characteristics

Output pulse width for OUT1 and OUT2	Modulation according DCF, 200 ms pulse	t_{WO200}	170	195	230	ms
Output pulse width for OUT1 and OUT2	Modulation according DCF, 100 ms pulse	t_{WO100}	70	95	130	ms

9 Test Circuitry with Pull-up Resistor (77.5 kHz)

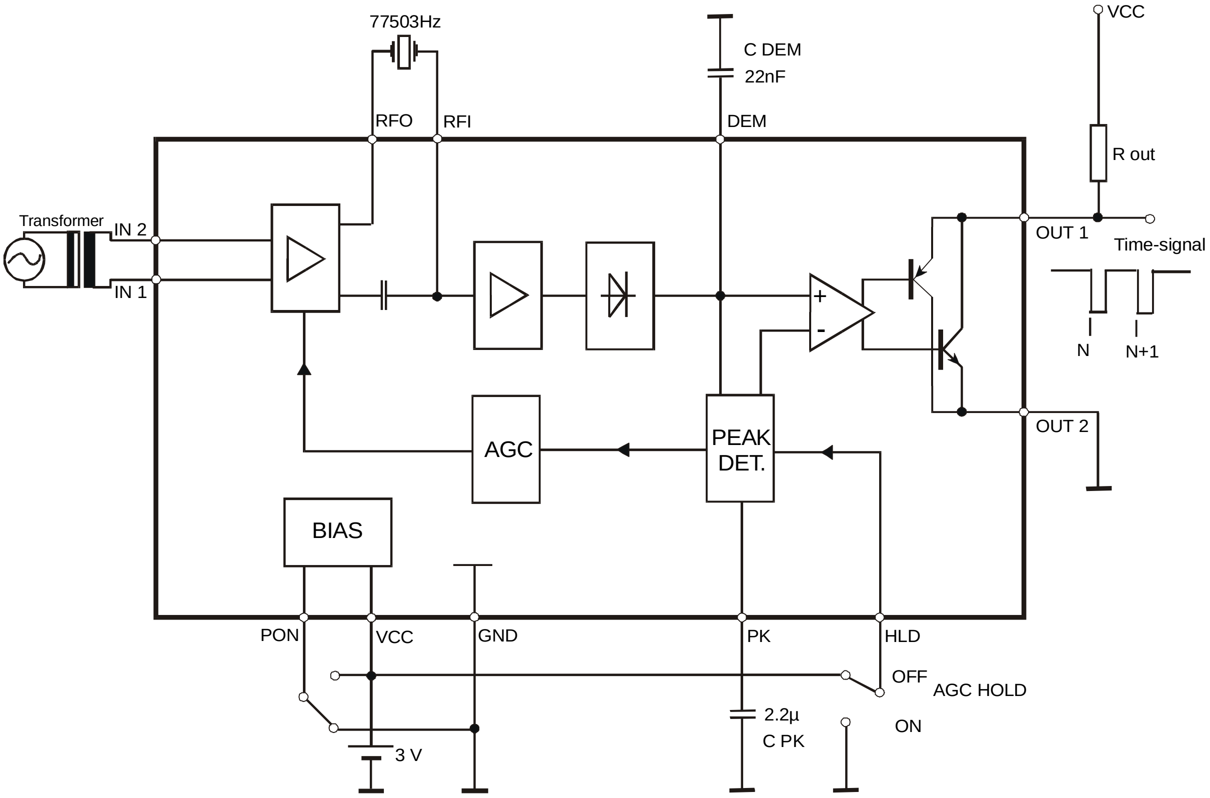


Figure 13. Test circuit

10 Test Circuitry with Pull-down Resistor (77.5 kHz)

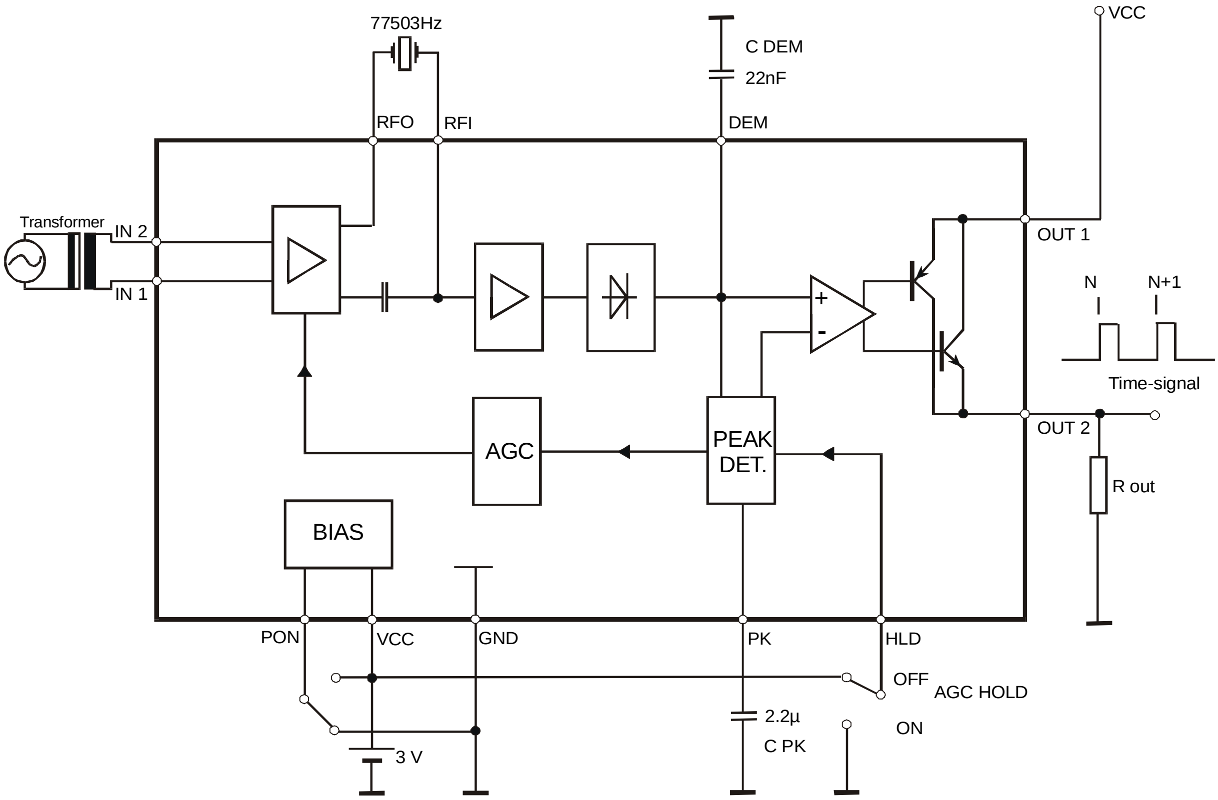


Figure 14. Test circuit

11 Application Circuitry with Pull-up Resistor

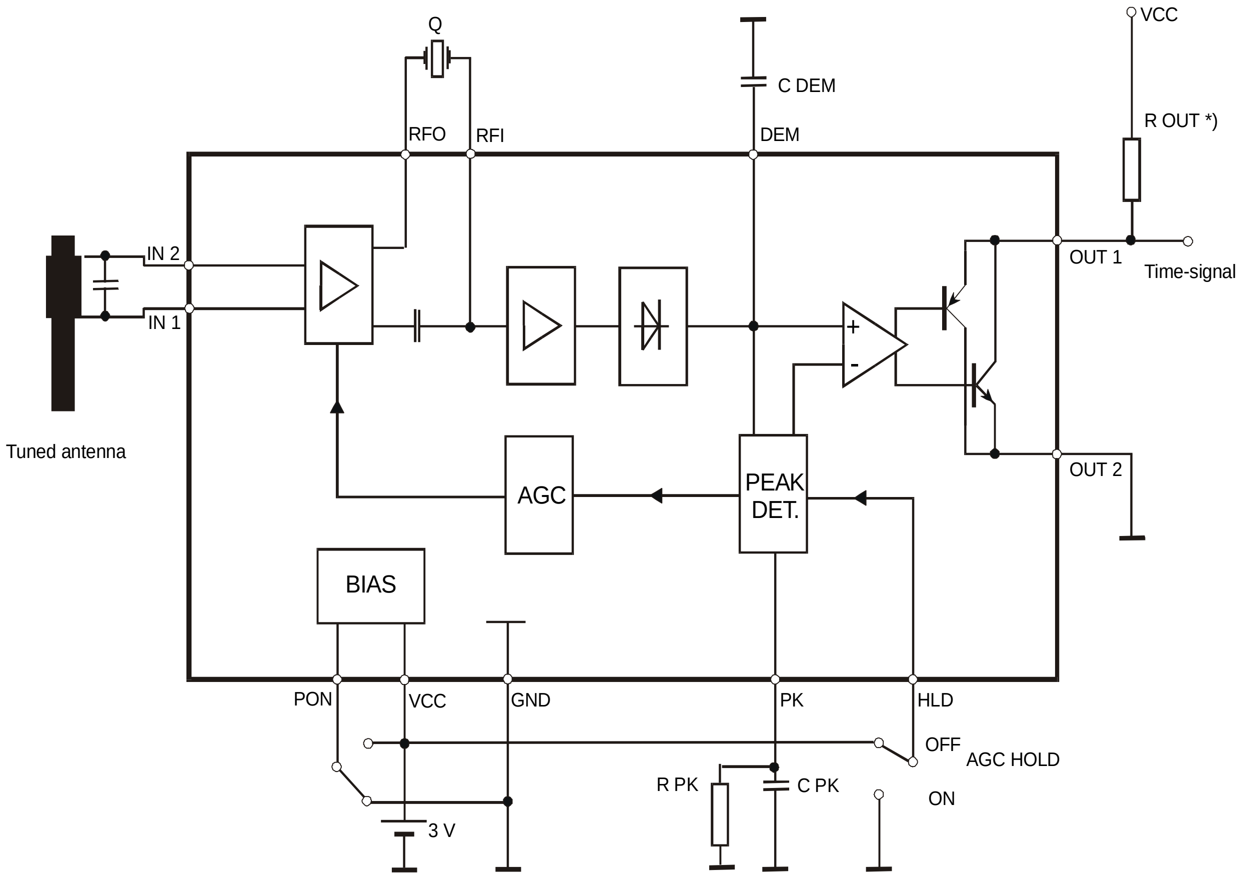


Figure 15. Application circuitry

Values of principle components in accordance with the carrier frequency of time-signal

Carrier frequency of time signal [Hz]	Data protocol of time signal	Q - Crystal [Hz]	C_{DEM} [nF]	C_{PK} [µF]	R_{PK} [MOhm]	R_{OUT} *) [kOhm]
40000	JJY	40000	100	4.7	-	≥100
60000	JJY; WWVB	60000	100	4.7	-	≥100
60000	MSF	60000	100	1	10	≥100
77500	DCF	77503	47	1	10	≥100

*) resistor Rout (≥100k) can be or an external discrete component or an integrated pull-up resistor of the connected controller-port

12 Information on the German Transmitter (Customer is responsible to verify this information)

Station:	DCF 77	Location:	Mainflingen/Germany
Frequency:	77.5 kHz	Geographical coordinates:	50° 01'N, 09° 00'E
Transmitting power:	50 kW	Time of transmission:	permanent

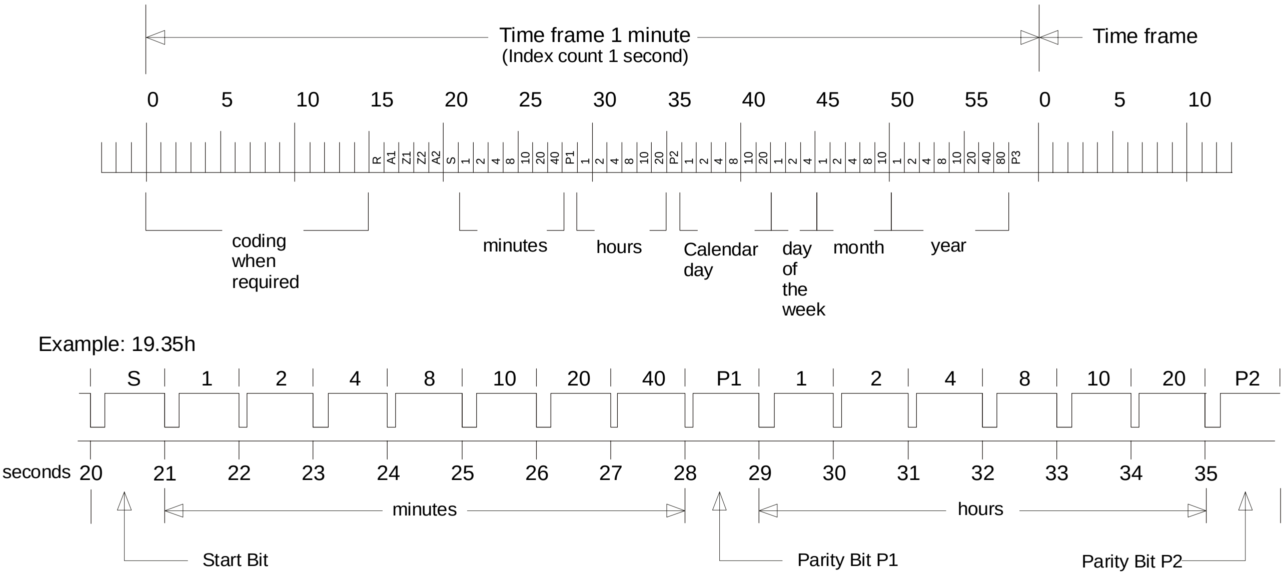


Figure 15.

Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

Time-Code Format (based on Information of Deutsche Bundespost)

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to summer time), Z1 (during summer time 200 ms, otherwise 100 ms), Z2 (during summer time 100 ms, otherwise 200 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

13 Information on the British Transmitter (Customer is responsible to verify this information)

Station:	MSF	Location:	Teddington, Middlesex
Frequency:	60 kHz	Geographical coordinates:	52° 22'N, 01° 11'W
Transmitting power:	50 kW	Time of transmission:	permanent, except the first Tuesday of each month from 10.00 h to 14.00 h.

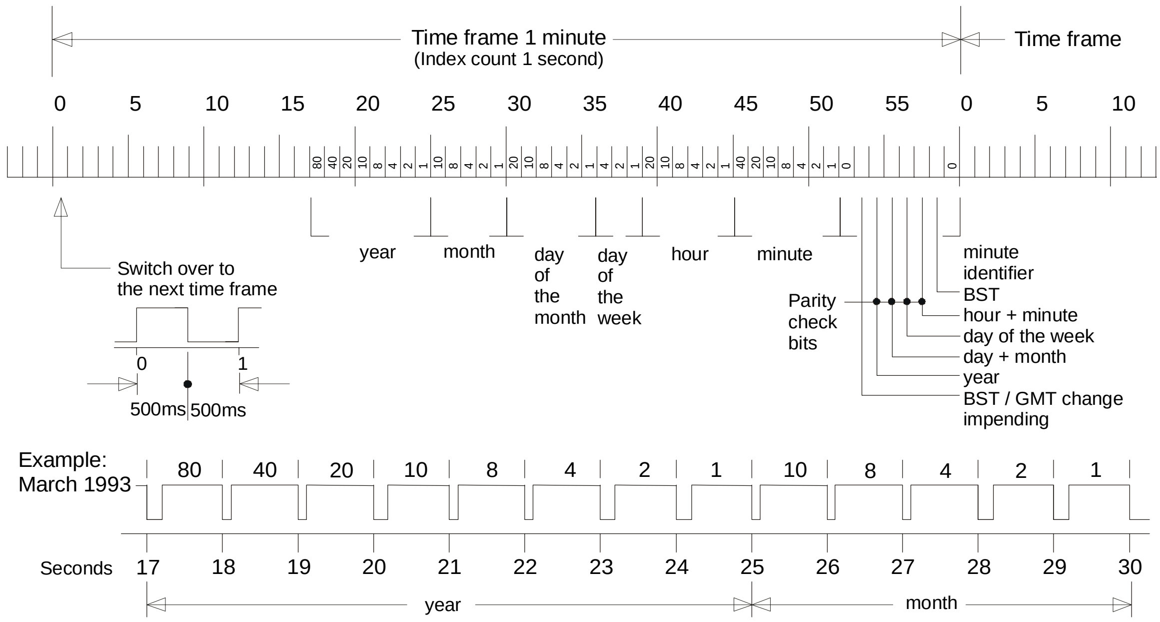


Figure 16.

Modulation

The carrier amplitude is switched off at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one).

Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is reduced for a period of 500 ms.
The presence of the fast code during the first 500 ms at the beginning of the minute is not guaranteed. The transmission rate is 100 bit/s and the code contains information of hour, minute, day and month.

14 Information on the US Transmitter (Customer is responsible to verify this information)

Station:	WWVB	Location:	Fort Collins/Colorado
Frequency:	60 kHz	Geographical coordinates:	40° 40'N, 105° 03' W
Transmitting power:	50 kW	Time of transmission:	permanent

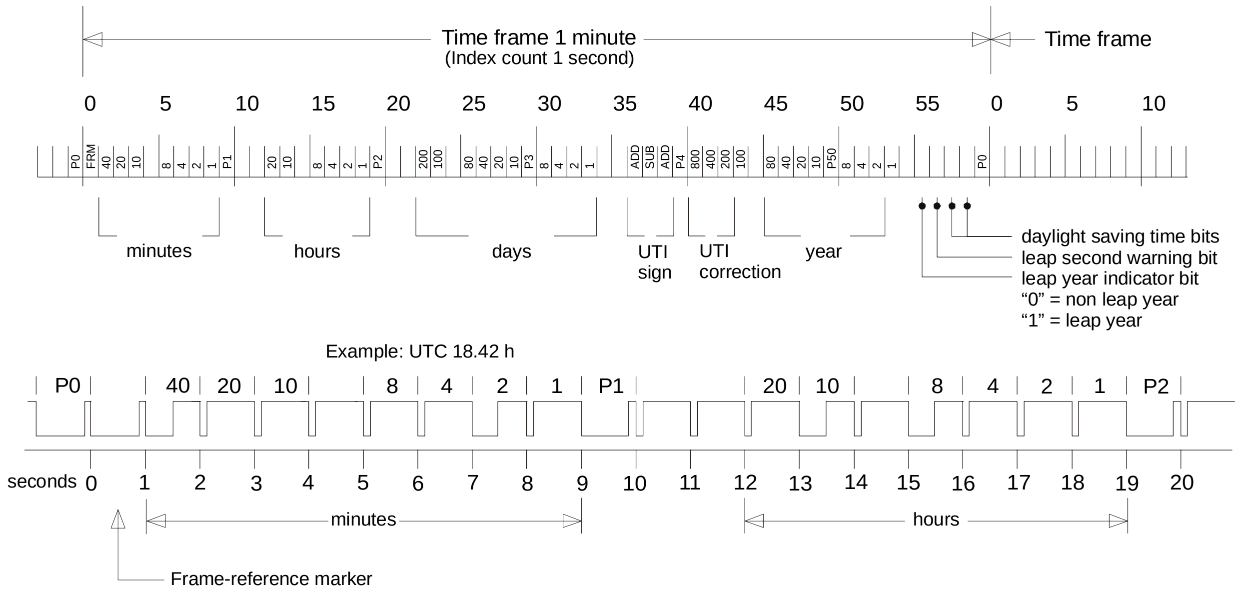


Figure 17.

Modulation

The carrier amplitude is reduced by 10 dB at the beginning of each second and is restored within 500 ms (binary one) or within 200 ms (binary zero) or within 800 ms (position-identifier marker or frame reference marker).

Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days and year. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference marker with reduced carrier amplitude of 800 ms duration

15 Information on the Japanese Transmitter (Customer is responsible to verify this information)

Station:	JJY	Location:	Sanwa Ibaraki
Frequency:	40 kHz	Geographical coordinates:	36° 11'N, 139° 51'E
Transmitting power:	10 kW	Time of transmission:	permanent

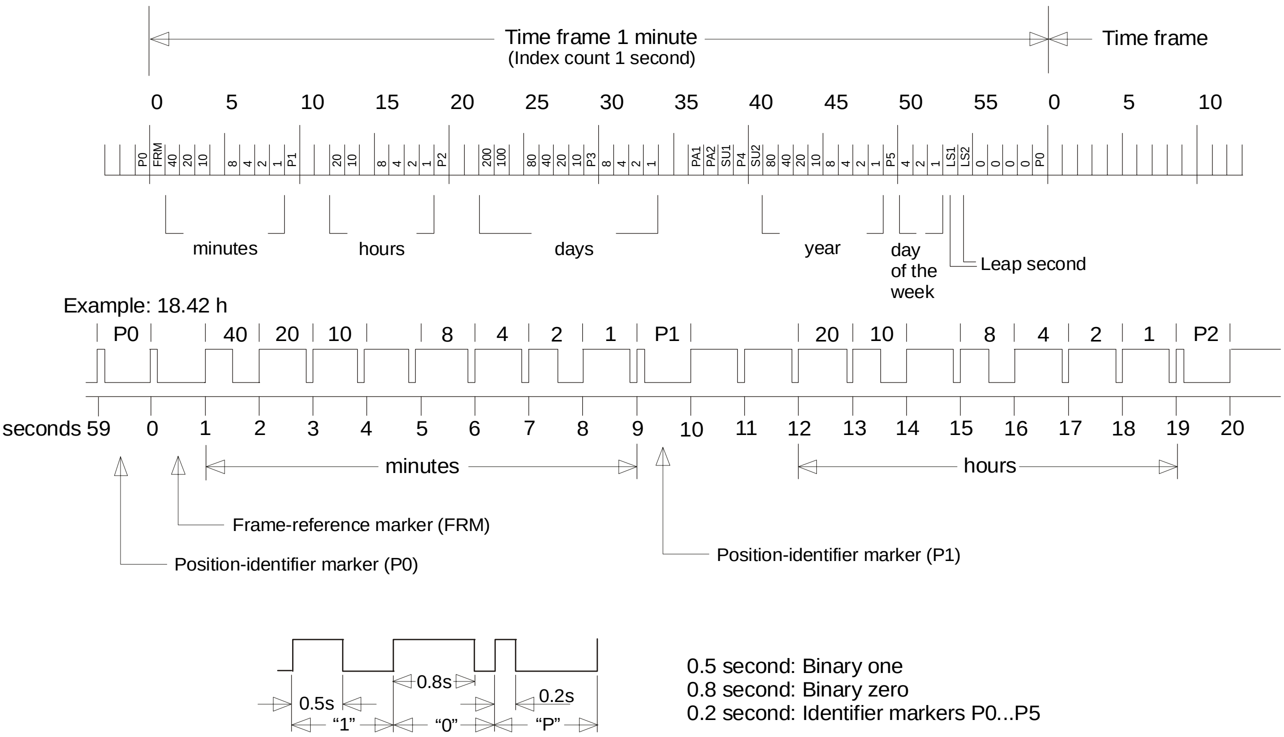


Figure 18.

Modulation

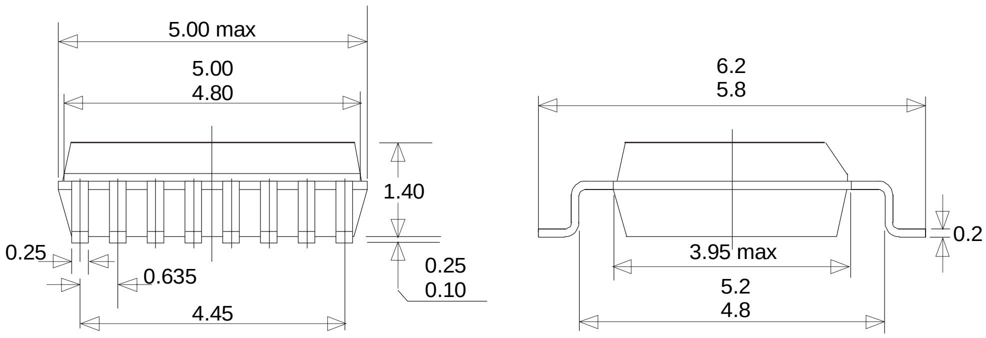
The carrier amplitude is 100% at the beginning of each second and is switched to 10% after 500 ms (binary one) or after 800 ms (binary zero) or after 200 ms for Position-identifier marker (P0...P5) and frame reference marker.

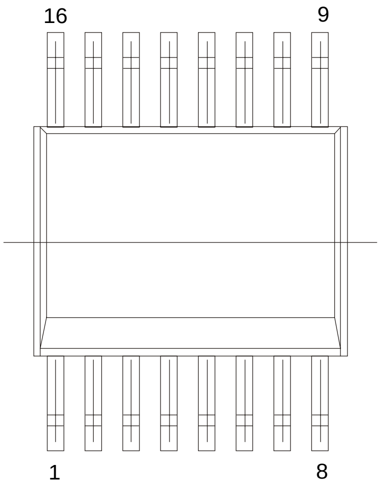
Time-Code Format

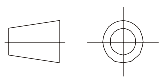
The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days, weeks and year. In addition, there are 6 position-identifier markers (P0 thru P5) with reduced carrier amplitude of 800 ms duration.

16 Package information

Package SSO16
Dimensions in mm







Technical drawings
according to DIN
specifications

17 Ozone Depleting Substances Policy Statement

It is the policy of **HKW Elektronik GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere, which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

HKW has been able to use the policy of continuous improvements to eliminate the use of ODSs listed in following documents.

1. Annex A,B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA.
3. Council Decision 88/540/EEC and 91/690/EEC Annex A,B and C (transitional substances) respectively.

HKW can certify that our semiconductor UE6005 is not manufactured with ozone depleting substances and do not contain such substances.

18 Disclaimer of Warranty

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The declared data are serving only to description of product. They are not guaranteed properties as defined by law. The examples are given without obligation and cannot given rise to any liability.

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