Description

The PBL 387 10/1 ring SLIC (Subscriber Line Interface Circuit) is a bipolar integrated circuit in 90 V technology which replaces the conventional transformer based analog line interface and ring relay in FITL, WLL, ISDN-TA and other telecommunications equipment with a modern, compact solid state design. Not only is required PCB area reduced, but less component weight and height result as well. The PBL 387 10/1 has been optimized for low cost and to require only a minimum of external components.

The PBL 387 10/1 constant-current feed system, programmable to max 40 mA of line current, can operate with battery supply voltages down to -21 V to reduce line card power dissipation.

The SLIC incorporates loop current, ground key and ring trip detection functions.

Two-to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter (e.g. SLAC, SiCoFi, Combo II). The programmable line terminating impedance could be complex or real to fit every market.

The PBL 387 10/1 package is 28-pin PLCC.

Key Features

- Ring SLIC eliminates ring relay and conventional ring-generator
- Supports sine wave and trapezoidal ringing
- -85 V battery feed for high voltage ring signal
- On chip automatic battery switch
- Programmable battery feed characteristics
- Battery supply voltage as low as -21 V for power efficient line card designs
- Low on-hook power dissipation, 50 mW @-24 V battery
- Loop current, ring trip and ground key detection functions
- Programmable loop current detector threshold
- Programmable ring trip detector threshold
- Hybrid function with all types of CODEC/filter devices
- Programmable line terminating impedance, complex or real
- On-hook transmission
- Tip-ring open circuit state for subscriber loop power denial

Figure 1. Block diagram.
### Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature, Humidity</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>$T_{stg}$</td>
<td>-55</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating junction temperature range</td>
<td>$T_J$</td>
<td>-40</td>
<td>+140</td>
<td>°C</td>
</tr>
<tr>
<td><strong>Power supply, -40°C ≤ $T_{Amb}$ ≤ 85°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ with respect to AGND</td>
<td>$V_{CC}$</td>
<td>-0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EE}$ with respect to AGND</td>
<td>$V_{EE}$</td>
<td>-6.5</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Bat}$ with respect to BGND</td>
<td>$V_{Bat}$</td>
<td>-85</td>
<td>$V_{EE} + 0.5$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Bat2}$ with respect to BGND</td>
<td>$V_{Bat2}$</td>
<td>$V_{Bat}$</td>
<td>$V_{EE} + 0.5$</td>
<td>V</td>
</tr>
<tr>
<td><strong>Power dissipation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous power dissipation at $T_{Amb}$ ≤ 85 °C</td>
<td>$P_D$</td>
<td>1.5</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Peak power dissipation at $T_{Amb}$ = 85 °C, $t &lt; 100$ ms, $t_{REP} &gt; 1$ sec.</td>
<td>$P_{DP}$</td>
<td>4</td>
<td></td>
<td>W</td>
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<tr>
<td><strong>Ground</strong></td>
<td></td>
<td></td>
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<tr>
<td>Voltage between AGND and BGND</td>
<td>$V_{G}$</td>
<td>-0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td><strong>Digital inputs, outputs</strong> (C1, C2, E1, HB, DET)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{ID}$</td>
<td>$V_{CC}$</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage (DET disabled)</td>
<td>$V_{OD}$</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Output current (DET enabled)</td>
<td>$I_{OD}$</td>
<td>5</td>
<td></td>
<td>mA</td>
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<tr>
<td><strong>Ring voltage, input (VR)</strong></td>
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<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{VR}$</td>
<td>$V_{EE}$</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td><strong>TIPX and RINGX terminals, -40°C ≤ $T_{Amb}$ ≤ 85°C, $V_{Bat} = -80$V, Active, Disconnect and Stand by states</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>TIPX or RINGX voltage, continuous (referenced to AGND), Note 1</td>
<td>$V_{TA}$, $V_{RA}$, $V_{Bat}$</td>
<td>2</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>TIPX or RINGX, pulse &lt; 10 ms, $t_{REP} &gt; 10$ s, Note 1</td>
<td>$V_{TA}$, $V_{RA}$, $V_{Bat}$</td>
<td>5</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>TIPX or RINGX, pulse &lt; 1 μs, $t_{REP} &gt; 10$ s, Note 1</td>
<td>$V_{TA}$, $V_{RA}$, $V_{Bat}$</td>
<td>25</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>TIP or RING, pulse &lt; 250 ns, $t_{REP} &gt; 10$ s, Note 1</td>
<td>$V_{TA}$, $V_{RA}$, $V_{Bat}$</td>
<td>35</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>TIPX or RINGX maximum current supplied</td>
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</tr>
<tr>
<td></td>
<td>$I_{TA}$</td>
<td>110</td>
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<td>mA</td>
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### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Ambient temperature</td>
<td>$T_{amb}$</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{CC}$ with respect to AGND</td>
<td>$V_{CC}$</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EE}$ with respect to AGND</td>
<td>$V_{EE}$</td>
<td>-5.25</td>
<td>-4.75</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Bat2}$ with respect to BGND, Note 2</td>
<td>$V_{Bat2}$</td>
<td>-58</td>
<td>-24</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Bat}$ with respect to BGND</td>
<td>$V_{Bat}$</td>
<td>-80</td>
<td>$V_{Bat2}$</td>
<td>V</td>
</tr>
</tbody>
</table>

### Notes
1. With diodes in series with the $V_{Bat}$ and $V_{Bat2}$, see figure 12.
2. $-24V < V_{Bat2} < -21V$ may be used in applications requiring maximum $V_f$ signal amplitudes less than $3V_{pk}$ (8.75 dBm, 600 Ω).
Electrical Characteristics

-40 °C ≤ T_{amb} ≤ 85 °C, V_{cc} = +5V ± 5 %, V_{ee} = -5V ± 5 %, V_{bat} = -80V, V_{bat2} = -48V, AGND = BGND, R_{dc1} = R_{dc2} = 41.7kΩ, R_{bgd} = 0Ω, R_{d} = 33kΩ, R_{or} = 5.8 kΩ, C_{hp} = 10nF, C_{dc} = 1.5 µF, Z_{L} = 600 Ω, state input control pin HB = 0, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ref figure</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-wire port</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overload level, V_{TRO}</td>
<td>2</td>
<td>Z_{L} = 600 Ω, 1% THD Note 1</td>
<td>3.1</td>
<td></td>
<td></td>
<td>V_{peak}</td>
</tr>
<tr>
<td>Input impedance, Z_{TR}</td>
<td>Note 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Longitudinal impedance, Z_{LT}, Z_{LR}</td>
<td>0 &lt; f &lt; 100 Hz</td>
<td>12</td>
<td>35</td>
<td></td>
<td>Ω/wire</td>
<td></td>
</tr>
<tr>
<td>Longitudinal current limit, I_{LT}, I_{LR}</td>
<td>active state</td>
<td>10</td>
<td></td>
<td></td>
<td>mA_{rms}/wire</td>
<td></td>
</tr>
<tr>
<td></td>
<td>stand-by state</td>
<td>8.5</td>
<td></td>
<td></td>
<td>mA_{rms}/wire</td>
<td></td>
</tr>
<tr>
<td>Longitudinal to metallic balance, B_{LM}</td>
<td>IEEE standard 455-1985</td>
<td>0.2 kHz ≤ f ≤ 1.0 kHz</td>
<td>46</td>
<td>63</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0 kHz ≤ f ≤ 3.4 kHz</td>
<td>46</td>
<td>58</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Longitudinal to metallic balance, B_{LME}</td>
<td>3</td>
<td>0.2 kHz ≤ f ≤ 1.0 kHz</td>
<td>46</td>
<td>63</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0 kHz ≤ f ≤ 3.4 kHz</td>
<td>46</td>
<td>58</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B_{LME} = 20 · Log \frac{E_{LR}}{V_{TR}}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Longitudinal to metallic balance, B_{LFE}</td>
<td>3</td>
<td>0.2 kHz ≤ f ≤ 1.0 kHz</td>
<td>46</td>
<td>63</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0 kHz ≤ f ≤ 3.4 kHz</td>
<td>46</td>
<td>58</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B_{LFE} = 20 · Log \frac{E_{LR}}{V_{TX}}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metallic to longitudinal balance, B_{MLE}</td>
<td>4</td>
<td>0.2 kHz &lt; f &lt; 3.4 kHz</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>B_{MLE} = 20 · Log \frac{V_{TR}}{V_{Lo}}, E_{RX} = 0</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Figure 2. Overload level, V_{TRO}, two-wire port

\[ \frac{1}{60 \text{kHz}} << R_{L}, R_{L} = 600 \text{ Ω} \]

\[ R_{T} = 600 \text{ kΩ}, R_{RX} = 300 \text{ kΩ} \]

Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

\[ \frac{1}{60 \text{kHz}} << 150 \text{ Ω}, R_{LT} = R_{LR} = 300 \text{ Ω} \]

\[ R_{T} = 600 \text{ kΩ}, R_{RX} = 300 \text{ kΩ} \]
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ref fig</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four-wire to longitudinal balance, $B_{FLE}$</td>
<td>4</td>
<td>$0.2 \text{ kHz} &lt; f &lt; 3.4 \text{ kHz}$</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$B_{FLE} = 20 \cdot \log \frac{</td>
<td>E_{RX}</td>
<td>}{E_{Lo}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Two-wire return loss, $r$</td>
<td></td>
<td>$r = 20 \cdot \log \frac{</td>
<td>Z_{TR} + Z_L</td>
<td>}{</td>
<td>Z_{TR} - Z_L</td>
<td>}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Z_{TR} = Z_L = \text{nom.} 600 \Omega$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0.2 \text{ kHz} \leq f \leq 0.5 \text{ kHz}$</td>
<td>25</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0.5 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$</td>
<td>27</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1.0 \text{ kHz} \leq f \leq 3.4 \text{ kHz}$, Note 9</td>
<td>23</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>TIPX idle voltage, $V_{Ti}$</td>
<td></td>
<td>active, $I_L = 0$</td>
<td>-1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>stand-by, $I_L = 0$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>RINGX idle voltage, $V_{Ri}$</td>
<td></td>
<td>active, $I_L = 0$</td>
<td>-46.5</td>
<td></td>
<td></td>
<td>V</td>
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<td></td>
<td></td>
<td>stand-by, $I_L = 0$</td>
<td>-47</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>TIPX-RINGX open loop metallic voltage, $V_{TR}$</td>
<td></td>
<td>$I_L = 0$, $R_{SG} = 0 \Omega$, $V_{Bat2} = -52V$</td>
<td>43.0</td>
<td>45.0</td>
<td>47.0</td>
<td>V</td>
</tr>
</tbody>
</table>

### Four-wire transmit port (VTX)

- **Overload level, $V_{TXO}$**
  - Ref fig: 5
  - Load impedance $> 20 \text{ k\Omega}$, $1\% \text{ THD}$, Note 3
  - $3.1 \text{ V}_{\text{Peak}}$

- **Output offset voltage, $\Delta V_{tx}$**
  - $-60 \text{ mV}$

- **Output impedance, $z_{TX}$**
  - $0.2 \text{ kHz} \leq f \leq 3.4 \text{ kHz}$
  - $< 5 \text{ Ohm}$

### Four-wire receive port (RSN)

- **Receive summing node (RSN) dc voltage**
  - $I_{RSN} = 0 \text{ mA}$
  - $0 \text{ V}$

- **Receive summing node (RSN) impedance**
  - $0.2 \text{ kHz} \leq f \leq 3.4 \text{ kHz}$
  - $< 10 \text{ Ohm}$

- **Receive summing node (RSN) current ($I_{RSN}$) to metallic loop current ($I_L$) gain, $\alpha_{RSN}$**
  - $0.3 \text{ kHz} \leq f \leq 3.4 \text{ kHz}$
  - $1000 \text{ ratio}$

---

**Figure 4. Metallic to longitudinal and four-wire to longitudinal balance**

$$\frac{1}{\omega C} \ll 150 \Omega, R_{LT} = R_{LR} = 300 \Omega$$

$$R_T = 600 \text{ k\Omega}, R_{RX} = 300 \text{ k\Omega}$$

**Figure 5. Overload level, $V_{TXO}$, four-wire transmit port**

$$\frac{1}{\omega C} \ll R_L, R_T = 600 \Omega$$

$$R_T = 600 \text{ k\Omega}, R_{RX} = 300 \text{ k\Omega}$$
### Frequency response

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-wire to four-wire, $g_{2,4}$</td>
<td>$0.3 \text{ kHz} &lt; f &lt; 3.4 \text{ kHz}$, relative to $0 \text{ dBm}$, $1.0 \text{ kHz}$, $E_{\text{rx}} = 0 \text{ V}$</td>
<td>-0.2</td>
<td>0.2</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Four-wire to two-wire, $g_{4,2}$</td>
<td>$0.3 \text{ kHz} &lt; f &lt; 3.4 \text{ kHz}$, relative to $0 \text{ dBm}$, $1.0 \text{ kHz}$, $E_{\text{l}} = 0 \text{ V}$</td>
<td>-0.2</td>
<td>0.2</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Four-wire to four-wire, $g_{4,4}$</td>
<td>$0.3 \text{ kHz} &lt; f &lt; 3.4 \text{ kHz}$, relative to $0 \text{ dBm}$, $1.0 \text{ kHz}$, $E_{\text{l}} = 0 \text{ V}$</td>
<td>-0.2</td>
<td>0.2</td>
<td>dB</td>
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### Insertion loss

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<th>Parameter</th>
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<th>Eqn</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Two-wire to four-wire, $G_{2,4}$</td>
<td>$0 \text{ dBm}$, $1.0 \text{ kHz}$, Note 4</td>
<td>$G_{2,4} = 20 \cdot \log \left( \frac{V_{\text{TX}}}{V_{\text{RX}}} \right)$, $E_{\text{RX}} = 0 \text{ V}$</td>
<td>-0.2</td>
<td>0.2</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Four-wire to two-wire, $G_{4,2}$</td>
<td>$0 \text{ dBm}$, $1.0 \text{ kHz}$, Notes 4, 5</td>
<td>$G_{4,2} = 20 \cdot \log \left( \frac{V_{\text{TR}}}{E_{\text{L}}} \right)$, $E_{\text{L}} = 0 \text{ V}$</td>
<td>-0.2</td>
<td>0.2</td>
<td>dB</td>
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### Gain tracking

<table>
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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Two-wire to four-wire</td>
<td>Ref. $-10 \text{ dBm}$, $1.0 \text{ kHz}$, Note 7</td>
<td>-0.1</td>
<td>0.1</td>
<td>dB</td>
<td></td>
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<tr>
<td>Four-wire to two-wire</td>
<td>Ref. $-10 \text{ dBm}$, $1.0 \text{ kHz}$, Note 8</td>
<td>-0.1</td>
<td>0.1</td>
<td>dB</td>
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### Noise

<table>
<thead>
<tr>
<th>Noise source</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Idle channel noise at two-wire</td>
<td>C-message weighting</td>
<td>10</td>
<td>12</td>
<td>dBmC</td>
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<tr>
<td>(TIPX-RINGX) or four-wire (VTX) output</td>
<td>Psophometrical weighting</td>
<td>-80</td>
<td>-78</td>
<td>dBmp</td>
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### Harmonic distortion

<table>
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<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Two-wire to four-wire</td>
<td>$0 \text{ dBm}$, $1.0 \text{ kHz}$ test signal</td>
<td>-60</td>
<td>dB</td>
</tr>
<tr>
<td>Four-wire to two-wire</td>
<td>$0.3 \text{ kHz} &lt; f &lt; 3.4 \text{ kHz}$</td>
<td>-60</td>
<td>dB</td>
</tr>
</tbody>
</table>

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**Note 6**

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**Figure 6. Frequency response, insertion loss, gain tracking.**

\[
\frac{1}{\omega C} \ll R_L, R_L = 600 \ \Omega
\]

\[
R_t = 600 \ \Omega, \ R_{\text{rx}} = 300 \ \Omega
\]
### Battery feed characteristics

**Constant loop current, \( I_{L_{\text{prog}}} \)**

\[
I_{L_{\text{prog}}} = \frac{2500}{R_{DC1} + R_{DC2}}, \quad R_{DC1}, R_{DC2} \text{ in k}\Omega
\]

\( 0.88 \, I_{L_{\text{prog}}}, \quad 1.12 \, I_{L_{\text{prog}}} \, \text{mA} \)

**Stand-by state loop current, \( I_L \)**

\[
I_L = \frac{|V_{\text{Bat}} - 2|}{R_L + 2000} ; \quad T_A = 25^\circ C
\]

\( 0.8 \, I_L, \quad 1.2 \, I_L \, \text{mA} \)

**Ring state loop current limit, \( I_{LLim} \)**

- \( V_{\text{TP-RING}} > 0 \, \text{V}, \, -40 \text{ to } 0 \, ^\circ \text{C} \)
  - \( 70 \, \text{mA} \)

- \( V_{\text{TP-RING}} < 0 \, \text{V}, \, -40 \text{ to } 0 \, ^\circ \text{C} \)
  - \( 47 \, \text{mA} \)

**Ring state loop current limit, \( I_{LLim} \)**

- \( V_{\text{TP-RING}} > 0 \, \text{V}, \, 0 \text{ to } 85 \, ^\circ \text{C} \)
  - \( 73 \, \text{mA} \)

- \( V_{\text{TP-RING}} < 0 \, \text{V}, \, 0 \text{ to } 85 \, ^\circ \text{C} \)
  - \( 50 \, \text{mA} \)

### Ring injection

**Input impedance, \( Z_{VR} \)**

\( R_L = 7 \, \text{k}\Omega, \, 1.1 \, \text{V} \leq VR \leq 1.9 \, \text{V} \)

\( 10.5 \, \text{k}\Omega \)

**Ring node (VR) voltage to tip-ring voltage (\( V_{\text{TR}} \)) gain**

20 Hz, DC

20 Hz, Sine

36.6, 38.6, 40.6

0.5, 2.5

### Loop current detector

**Loop current detector threshold**

\( I_{LTn} = 360 / R_D \), \( R_D = 33 \, \text{k}\Omega \)

\( 0.85 \, I_{LTn}, \quad 1.15 \, I_{LTn} \, \text{mA} \)

### Ground key detector

**I_{LTIPX} \text{ and } I_{RINGX} current difference, \Delta I_{LOn} \text{, to trigger the ground key detector**

5.5, 10.5, 15.5

### Ring trip detector

**Ring trip detector threshold**

\( I_{RTn} = 360 / R_{DR} \), \( R_{DR} = 5.8 \, \text{k}\Omega \)

\( 0.85 \, I_{RTn}, \quad 1.15 \, I_{RTn} \, \text{mA} \)

### Digital inputs (C1, C2, HB, E1)

**Input low voltage, \( V_{IL} \)**

0, 0.8

\( \text{V} \)

**Input high voltage, \( V_{IH} \)**

2.0

\( V_{CC} \)

**Input low current, \( I_{IL} \)**

- C1, C2, HB
  - \( V_L = 0.4 \, \text{V} \)
  - \(-700 \, \mu\text{A} \)

- E1
  - \(-100 \, \mu\text{A} \)

**Input high current, \( I_{IH} \)**

\( V_{IH} = 2.4 \, \text{V} \)

200

\( \mu\text{A} \)

### Detector output (DET)

**Output low voltage, \( V_{DL} \)**

\( I_{DL} = 2 \, \text{mA} \)

0.45

\( \text{V} \)

**Output high voltage, \( V_{DH} \)**

\( I_{DH} = 100 \, \mu\text{A} \)

2.7

\( \text{V} \)

**Internal pull-up resistor**

\( 7.0, 15.6, 27.0 \, \text{k}\Omega \)

### Power dissipation (\( V_{\text{Bat}} = -48\text{V} \))

**\( P_1 \)**

Open circuit state, C1, C2 = 0, 0

35, 60

\( \text{mW} \)

**\( P_2 \)**

Stand-by state, HB = 0

C1, C2 = 1, 1; on-hook

60, 100

\( \text{mW} \)

**\( P_3 \)**

Active state, C1, C2 = 0, 1

On-hook, \( R_L = \infty \) @ \( V_{\text{Bat}} = -24\text{V} \)

130

\( \text{mW} \)

**\( P_4 \)**

Off-hook, \( R_L = 300 \, \Omega \) @ \( V_{\text{Bat}} = -24\text{V} \)

610

\( \text{mW} \)
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ref</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply currents</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ current, $I_{CC}$</td>
<td>Open circuit state</td>
<td>2.0</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EE}$ current, $I_{EE}$</td>
<td>C1, C2 = 0, 0</td>
<td>1.2</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat}$ current, $I_{Bat}$</td>
<td>On-hook</td>
<td>0.2</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat2}$ current, $I_{Bat2}$</td>
<td>0.1</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ current, $I_{CC}$</td>
<td>Stand-by state</td>
<td>2.4</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EE}$ current, $I_{EE}$</td>
<td>C1, C2 = 1, 1</td>
<td>1.1</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat}$ current, $I_{Bat}$</td>
<td>On-hook</td>
<td>0.4</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat2}$ current, $I_{Bat2}$</td>
<td>0.3</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ current, $I_{CC}$</td>
<td>Active state</td>
<td>5.9</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EE}$ current, $I_{EE}$</td>
<td>C1, C2 = 0.1</td>
<td>2.3</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat}$ current, $I_{Bat}$</td>
<td>On-hook</td>
<td>0.2</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat2}$ current, $I_{Bat2}$</td>
<td>$V_{Bat} = -80\text{V}, V_{Bat2} = -24\text{V}$</td>
<td>3.1</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply rejection ratios</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ to 2- or 4-wire port</td>
<td>Active State</td>
<td>45</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EE}$ to 2- or 4-wire port</td>
<td>C1, C2 = 0.1</td>
<td>45</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat}$ to 2- or 4-wire port</td>
<td>50Hz &lt; f &lt; 3400Hz, $V_{n} = 100mV_{RMS}$</td>
<td>32</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Bat2}$ to 2- or 4-wire port</td>
<td>45</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature guard</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction threshold temperature, $T_{JG}$</td>
<td></td>
<td>160</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin PLCC, $\theta_{RIP28plcc}$</td>
<td>Junction to terminals 3, 10, 17, 24 connected together</td>
<td>20</td>
<td>°C/W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   \[ Z_{TRX} = Z_{r} | G_{2-4} \cdot \alpha_{RSN} | \]
   where:
   - $Z_{TRX} =$ impedance between the TIPX and RINGX terminals
   - $Z_{r} =$ programming network between the VTX and RSN terminals
   - $G_{2-4} =$ transmit gain, nominally = 1
   - $\alpha_{RSN} =$ receive current gain, nominally = -1000 (current defined as positive when flowing into the receive summing node (RSN), and when flowing from Tip to Ring).
3. The overload level is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4} = 1$.
4. Fuse resistors $R_{F}$ impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for $R_{F} = 0$.
5. The specified insertion loss tolerance does not include errors caused by external components.
6. The two-wire idle noise is specified with the port terminated in $600 \ \Omega \ (R_{L})$ and with the four-wire receive port grounded ($E_{RX} = 0$). The four-wire idle noise at VTX is specified with the two-wire port terminated in $600 \ \Omega \ (R_{L})$. The noise specification is with respect to a $600 \ \Omega$ programmed two wire impedance level at VTX. The four-wire receive port is grounded ($E_{RX} = 0$).
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a $600 \ \Omega$ programmed two wire impedance level.
9. Higher return loss values can be achieved by adding a reactive component to $R_{t}$, the two-wire terminating impedance programming resistance, e.g., by dividing $R_{t}$ into two equal halves and connecting a capacitor from the common point to ground. For $R_{t} = 600 \ \text{k}\Omega$ this capacitor would be approximately 30 pF. Increasing $C_{HP}$ to 0.033 μF improves low-frequency return loss.
Figure 8. Pin configuration 28-pin PLCC, top view.

* Pin must be left open
## Pin Description

Refer to figure 8.

<table>
<thead>
<tr>
<th>PLCC</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BGND</td>
<td><strong>Ground</strong>. Should be tied together with AGND.</td>
</tr>
<tr>
<td>2</td>
<td>VBAT2</td>
<td>Low <strong>battery</strong> supply voltage.</td>
</tr>
<tr>
<td>3</td>
<td>VBAT</td>
<td>High <strong>battery</strong> supply voltage.</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>+5V power supply</td>
</tr>
<tr>
<td>5</td>
<td>HB</td>
<td>Enables the <strong>High battery</strong> to be present in the stand-by state. The purpose is to be able to offer a high open-loop voltage (battery switch between ring and active state is controlled from the control pins).</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td><strong>No internal Connection. Note 1.</strong></td>
</tr>
<tr>
<td>7</td>
<td>VR</td>
<td><strong>Voltage Ring.</strong> Low voltage (2Vpk) ringsignal (any waveform) is injected here.</td>
</tr>
<tr>
<td>8</td>
<td>RSG</td>
<td>The internal <strong>Saturation Guard programming Resistor, R\textsubscript{SG},</strong> connects from this terminal to VEE. Refer to section &quot;Battery feed&quot; for detailed information.</td>
</tr>
<tr>
<td>9</td>
<td>E1</td>
<td>TTL compatible <strong>Enable input.</strong> Enables desired detector to be gated to the DET output. Refer to section &quot;Control inputs&quot; for detailed information.</td>
</tr>
<tr>
<td>10</td>
<td>VBAT</td>
<td>This pin is used for heat sinking and is internally connected to VBAT.</td>
</tr>
<tr>
<td>11</td>
<td>DET</td>
<td>Detector output. Inputs C1 and C2 together with enable input E1 select one of the three detectors to be connected to the DET output. A logic low at the enabled DET output indicates a triggered detector condition. The DET output is open collector with internal pull-up resistor (approximately 15 k(\Omega) to V(\text{CC})).</td>
</tr>
<tr>
<td>12</td>
<td>C2</td>
<td>C1 and C2 are TTL compatible inputs controlling the SLIC operating states.</td>
</tr>
<tr>
<td>13</td>
<td>C1</td>
<td>Refer to section &quot;Control inputs&quot; for details.</td>
</tr>
<tr>
<td>14</td>
<td>RDC</td>
<td>Constant current feed is programmed by two resistors connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to GND to isolate the ac signal components.</td>
</tr>
<tr>
<td>15</td>
<td>AGND</td>
<td><strong>Ground.</strong> Should be tied together with BGND.</td>
</tr>
<tr>
<td>16</td>
<td>RSN</td>
<td>Receive summing node. 1000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for constant current feed, two-wire impedance and receive gain connect to the receive summing node.</td>
</tr>
<tr>
<td>17</td>
<td>VBAT</td>
<td>This pin is used for heat sinking and is internally connected to pin 3.</td>
</tr>
<tr>
<td>18</td>
<td>VEE</td>
<td>-5V power supply.</td>
</tr>
<tr>
<td>19</td>
<td>VTX</td>
<td>Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one. The two-wire impedance programming network connects between VTX and RSN.</td>
</tr>
<tr>
<td>20</td>
<td>HPT</td>
<td>Tip side of ac/dc separation capacitor C(\text{hp}). Other end of C(\text{hp}) capacitor connects to pin HPR.</td>
</tr>
<tr>
<td>21</td>
<td>HPR</td>
<td>Ring side of ac/dc separation capacitor C(\text{hp}). Other end of C(\text{hp}) connects to pin HPT.</td>
</tr>
<tr>
<td>22</td>
<td>RD</td>
<td><strong>Off-hook detector Programming Resistor R\textsubscript{D},</strong> in parallel with filter capacitor C(\text{D}), connect from RD to VEE.</td>
</tr>
<tr>
<td>23</td>
<td>RDR</td>
<td>Connect to the &quot;ring trip detector&quot; resistor.</td>
</tr>
<tr>
<td>24</td>
<td>VBAT</td>
<td>This pin is used for heat sinking and is internally connected to pin 3.</td>
</tr>
<tr>
<td>25</td>
<td>NC</td>
<td><strong>No internal Connection. Note 1.</strong></td>
</tr>
<tr>
<td>26</td>
<td>TIPX</td>
<td>The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components.</td>
</tr>
<tr>
<td>27</td>
<td>RINGX</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>NC</td>
<td><strong>No internal Connection. Note 1.</strong></td>
</tr>
</tbody>
</table>

**Note:**

1. Terminals marked NC are not internally connected to the chip but may be used for future functions. Do leave open.
A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

\[ V_{TR} = V_{TX} + I_L \cdot 2R_F \quad (1) \]

\[ V_{TX} + V_{RX} = \frac{I_L}{Z_T} \cdot \frac{1}{1000} \quad (2) \]

\[ V_{TR} = E_L - I_L \cdot Z_L \quad (3) \]

where:

- \( V_{TX} \) is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.
- \( V_{TR} \) is the ac metallic voltage between tip and ring.
- \( E_L \) is the line open circuit ac metallic voltage.
- \( I_L \) is the ac metallic current.
- \( R_F \) is a fuse resistor.
- \( Z_T \) is the line impedance.
- \( Z_L \) determines the SLIC TIPX to RINGX impedance at voice frequencies.
- \( Z_{RX} \) controls four- to two-wire gain.
- \( V_{RX} \) is the analog ground referenced receive signal.

**Functional Description and Applications Information**

**Transmission**

**General**

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

\[ V_{TR} = V_{TX} + I_L \cdot 2R_F \quad (1) \]

\[ \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{1000} \quad (2) \]

\[ V_{TR} = E_L - I_L \cdot Z_L \quad (3) \]

where:

- \( V_{TX} \) is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.
- \( V_{TR} \) is the ac metallic voltage between tip and ring.
- \( E_L \) is the line open circuit ac metallic voltage.
- \( I_L \) is the ac metallic current.
- \( R_F \) is a fuse resistor.
- \( Z_T \) is the line impedance.
- \( Z_{RX} \) controls four- to two-wire gain.
- \( V_{RX} \) is the analog ground referenced receive signal.

**Two-Wire Impedance**

To calculate \( Z_{TR} \), the impedance presented to the two-wire line by the SLIC, in active state, including the fuse resistor \( R_F \), let \( V_{RX} = 0 \).

From (1) and (2):

\[ Z_{TR} = \frac{Z_T}{1000} + 2R_F \]

Thus with \( Z_{TR} \) and \( R_F \) known:

\[ Z_T = 1000 \cdot (Z_{TR} - 2R_F) \]

The SLICs two-wire output impedance in ringing state is typically 2 - 40 \( \Omega \) for a 15 - 100 Hz ring-signal.

**Two-Wire to Four-Wire Gain**

From (1) and (2) with \( E_L = 0 \):

\[ G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T}{1000} \cdot \frac{1}{Z_T + 2R_F} \]

**Four-Wire to Four-Wire Gain**

From (1), (2) and (3) with \( E_L = 0 \):

\[ G_{4-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T}{Z_{RX}} \cdot \frac{Z_T + 2R_F}{Z_T + Z_L + 2R_F} \]

**Hybrid Function**

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance \( Z_b \) a current proportional to \( V_{RX} \) is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to \( V_{RX} \) is returned to \( V_{TX} \). This voltage is converted by \( R_{TX} \) to a current flowing into the same summing node. These currents can be made to cancel by letting:

\[ \frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_b} = 0 \quad (E_L = 0) \]

The four-wire to four-wire gain, \( G_{4-4} \), includes the required phase shift and thus the balance network \( Z_b \) can be calculated from:

\[ Z_b = \frac{Z_T}{R_{TX} \cdot Z_{RX} \cdot \frac{1000}{Z_T + Z_L + 2R_F}} \]

If calculation of the \( Z_b \) formula above yields a balance network containing an inductor, an alternate method is recommended. Contact Ericsson Microelectronics for assistance.

The PBL 38710/1 SLICs may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.
Longitudinal Impedance

A feedback loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, $V_{L0Ref}$.

$$V_{L0} = I_{Lo} \frac{R_{Lo}}{1000}$$

which reduces to

$$R_{LoT} = R_{LoR} = \frac{V_{Lo}}{I_{Lo}} = 20k\Omega/1000 = 20\Omega$$

where $R_{Lo}$ is the longitudinal resistance/wire.

$V_{Lo} =$ longitudinal voltage at TIPX, RINGX

$I_{Lo} =$ longitudinal current

$V_{LoRef} = \frac{V_{Bat2} + V_{Ring}}{2}$

where $V_T$ and $V_R$ are tip and ring ground referenced voltages without any longitudinal component. As shown below the SLIC appears as 20 $\Omega$ per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. Refer to figure 11.

Circuit analysis yields:

$$V_{Lo} = I_{Lo} \frac{R_{Lo}}{1000}$$

Capacitors $C_{TC}$ and $C_{RC}$

The capacitors designated $C_{TC}$ and $C_{RC}$ in figure 12, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the active components in the overvoltage protection network before they have had time to activate and could damage the SLIC. $C_{TC}$ and $C_{RC}$ short such very fast transients to ground. $C_{TC}$ and $C_{RC}$ also work as RFI-filters in conjunction with suitable series impedances (i.e., resistances, inductances). Resistors $R_{F1}$ and $R_{F2}$ may be sufficient, but series inductances can be added to form a second order filter. The recommended value for $C_{TC}$ and $C_{RC}$ is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. $C_{TC}$ and $C_{RC}$ contribute to a metallic impedance of $1/(\pi f C_{TC})$, a TIPX to ground impedance of $1/(2\pi f C_{TC})$ and a RINGX to ground impedance of $1/(2\pi f C_{RC})$.

AC - DC Separation Capacitor, $C_{HP}$

The high pass filter capacitor connected between terminals HPT and HPR provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A $C_{HP}$ value of 10 nF will position the low end frequency response 3dB break point at 48 Hz ($f_{3dB}$) according to $f_{3dB} = 1/(2\pi R_{HP} C_{HP})$ where $R_{HP} = 330$ k$\Omega$.

Battery Feed

The block diagram in figure 13 shows the PBL 38710/1 battery feed system and figure 14 illustrates the battery feed characteristics in the active state.

For a tip to ring dc voltage $V_{TR}$ less than the saturation guard reference voltage $V_{SGRef}$, the SLIC emulates a constant current feed characteristic in the active state. The constant current is independent of the actual battery voltage, $V_{Bat2}$, connected to the SLIC.

With the tip to ring DC voltage $V_{TR}$ exceeding $V_{SGRef}$, the feed characteristic changes to a nearly-constant voltage feed. This is to prevent the tip and ring drive amplifiers from distorting the AC signal as might have otherwise occurred due to insufficient voltage margin between $V_{TR}$ and $V_{Bat2}$. Thus the SLIC
Figure 12. Single-channel subscriber line interface with PBL 378 10/1 and combination CODEC/filter.

Figure 13. Battery feed (C2, C1 = 1, 0 active state).
automatically adjusts the tip to ring dc voltage $V_{TR}$ to the maximum safe value.

With the SLIC in the stand-by state ($C2,C1=1.1$) a resistiv feed characteristic is enabled. To achieve a high open loop voltage it is possible to switch the battery feed from $V_{Bat2}$ to $V_{Bat}$.

When the SLIC is in the ringing state $V_{Bat}$ is used in order to achieve a ring voltage as high as possible. The battery feed programming is also disconnected.

The following text explains the four battery cases in more detail.

**Case 1: SLIC in the active state**

$V_{TR} < V_{SGRef}$

In the active state $C2=1$, $C1=0$ and $V_{Bat}$ is used for battery feed. In this operating state tip to ring voltages $V_{TR}$ less than $V_{SGRef}$ cause the block titled saturation guard (figure 13) to be disabled, i.e. its output is equal to zero.

For this case circuit analysis yields:

$$R_{DC1} + R_{DC2} = \frac{2.5}{I_{Prog}} \cdot 1000$$

where:

$I_{Prog} =$ constant loop current (independent of the loop resistance $R_L$).

$R_{DC1} + R_{DC2} =$ the programming resistance which sets the constant loop current.

For a tip to ring voltage $V_{TR}$ less than $V_{SGRef}$ the PBL 38710/1 thus emulate a constant current feed with the magnitude of the constant current set by resistors, $R_{DC1}$ and $R_{DC2}$.

Capacitor $C_{DC}$ at the $R_{DC1} - R_{DC2}$ common point removes rf signals from the battery feed control loop. $C_{DC}$ is calculated according to:

$$C_{DC} = T \cdot \left( \frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right)$$

where $T=30$ ms. Note that $R_{DC1}=R_{DC2}$ yields minimum $C_{DC}$ value.

**Case 2: SLIC in the active State**

$V_{TR} > V_{SGRef}$

In the active state $C2=1$, $C1=0$ and $V_{Bat}$ is used for battery feed. The saturation guard reference voltage is user programmable according to:

$$V_{SGRef} = 12.9 + \frac{4.9 \cdot 10^5}{17300 + R_{SG}}$$

where:

$R_{SG} =$ saturation guard reference programming resistor in $\Omega$.

$V_{SGRef} =$ saturation guard reference voltage in volts.
Case 3: SLIC in the Stand-by State

In the stand-by state C1=1, C2=1 and input HB selects the battery to be used for battery feed. With the SLIC operating in the stand-by, power saving state, the tip and ring drive amplifiers are disconnected and a resistive battery feed is engaged. The loop current can be calculated from:

\[
I_L = \frac{|V_{BA|} - 2}{R_L + 2000}
\]

where:

- \( I_L \) = loop current (A).
- \( R_L \) = loop resistance (Ω).
- \( V_{BA|} \) = battery supply voltage \( V_{BA2} \) or \( V_{BA2} \) depends on input HB (V).

The stand-by short circuit loop current \( I_{LSH} \) for \( V_{BA2} = -28V \) (HB=0) is then limited to:

\[
I_{LSH} = 13.9 mA.
\]

HB=1 enables \( V_{BA} \) for use in applications that demand a high open loop voltage. Note that the equation above is also valid in the high battery voltage condition where the SLIC will not change to active state by itself when the loop current detector goes low. Switching between stand-by and active state is controlled via inputs C1 and C2.

Case 4: SLIC in the Ringing State

In the ringing state C2=0, C1=1 and \( V_{BA} \) is used for battery feed. To calculate loop current during ringing, see the "PBL 38710/1 Power Dissipation" section.

PBL 38710/1 Power Dissipation

Two cases: active \( V_{BA2} \) is used for battery feed) and ringing \( V_{BA} \) is used for battery feed).

The short circuit SLIC power dissipation is (in active state):

\[
P_{SLIC} = I_{LSH} \left( \left| V_{BAT2} \right| - 2R_F \right) + P_3
\]

where \( V_{BA2} \) is the battery voltage connected to the SLIC at pin VBAT2.

\[
I_{LSH} = \frac{2.5 \cdot 1000}{R_{DC1} + R_{DC2}}
\]

is the constant loop current. \( P_3 \) is on hook active state power dissipation (typ 130mW; \( V_{BA2} = -24V \)). Note that a short circuited loop is not a normal operational condition. The terminal equipment will add some dc resistance (typically 150 to 300 Ω) even if the wire resistance is close to 0 Ω. Figure 23 compares line feed power dissipation as a function of loop resistance for three cases: feed resistor dissipation for a conventional 2-400 Ω resistive feed, PBL 38710/1 with 30 mA constant current feed and \( V_{BAT2} = -48V \) and PBL 38710/1 with 30 mA constant current feed and \( V_{BAT2} = -28V \). The diagram illustrates the significant PBL 38710/1 power-saving compared to the 2-400 Ω feed.

During ringing the highest power dissipation occurs when the line is 0 Ω and maximum number of bells are connected (5REN). For information about the REN specification see the "Ring Voltage" section. The line current is calculated as:

\[
P_{SLIC} = I_{LSH} \cdot (|V_{BA2}| - 3Z_{BAT} + Z_{LINE} + 2R_F + Z_{TR})
\]

where:

- \( Z_{BAT} \) = bell impedance.
- \( Z_{LINE} \) = line impedance.
- \( R_F \) = fuse and protection resistors.
- \( Z_{TR} \) = tip-ring impedance during ringing (typically 2-40 Ω).

The maximum SLIC power dissipation during ringing is calculated as:

\[
P_{SLIC} = P_S \cdot P_{OUT}
\]

where (for a sinusoidal shaped ring-signal)

\[
P_S = 2 \cdot \frac{V_{BAT}}{\pi} \cdot I_{MAX} + P_{TROpen}
\]

and

\[
P_{OUT} = I_{LMS} \cdot (Z_{Bell} + 2R_F)
\]

Example: calculate the maximum slc power dissipation when \( V_{BAT} = -80V \), \( Z_{Bell} = 1.4 \Omega\) (SUSREGEN), \( Z_{LINE} = 0 \), \( R_F = 40 \Omega \) and \( Z_{TR} = 2-40 \Omega \). For these component values \( I_{MAX} = 47 mA \), \( P_S = 2.8 W \) (\( P_{TROpen} = 390 mW \) typ) @ \( V_{BAT} = -80V \) in ringing state), \( P_{OUT} = 1.7 W \) and \( P_{SLIC} = 1.1 W \) which is less than the maximum allowed power dissipation (\( P_D = 1.5 W \), see data sheet).

Temperature Guard

A ring to ground short circuit fault condition as well as other improper operating conditions may cause excessive SLIC power dissipation. If junction temperature increases beyond \( T_J \), the junction threshold temperature, the temperature guard will trigger, causing the SLIC to be set to a high-impedance state. In this high impedance state, power dissipation is reduced and
the junction temperature will return to a safe value. Once below $T_{JG}$, the SLIC is returned back to its normal operating mode and will remain in that state, assuming the fault condition has been removed. As long as the temperature guard is triggered, the loop current detector will stay in active state.

PBL 38710/1 Long Loop$\text{vf}$ Transmission

To ensure that the maximum $\text{vf}$ signal intended to be received/transmitted by the SLIC will not experience limiting in the TIPX / RINGX drive amplifiers at long loops, the saturation guard must be correctly programmed. The section, “Battery Feed, Case 2” describes how to calculate a value for the saturation guard programming resistor $R_{SG}$.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, $\text{DET}$. The detector to be connected to $\text{DET}$ is selected via the control inputs. Please refer to section Control Inputs for a description of the control interface.

Loop Current Detector

The loop current detector is indicating that the telephone is off hook by putting the $\text{DET}$ output to a logical low level when selected. The loop current threshold value, $I_{LTh}$, at which the loop current detector changes state is programmable by selecting the value of resistor $R_D$. $R_D$ connects between pin RD and VEE.

Figure 15 shows a block diagram of the loop current detector. The two-wire interface produces a current flowing out of the pin RD:

$$I_{RD} = \frac{|I_{LTIPX} - I_{LRINGX}|}{600} = I_L / 300$$

where $I_{LTIPX}$ and $I_{LRINGX}$ are currents flowing into the TIPX and RINGX terminals and $I_L$ is the loop current. The voltage generated by $I_{RD}$ across the programming resistor $R_D$ is compared to an internal reference by a comparator. A logic low results at the $\text{DET}$ output when the loop current exceeds the on-hook to off-hook detect threshold, $I_{LTh}$.

The programming resistor, $R_D$, can be calculated for a desired $I_{LTh}$ from:

$$R_D = \frac{360}{I_{LTh}}$$

$R_D$ is in kΩ for $I_{LTh}$ in mA. When the loop current is less than $I_{LTh}$, the $\text{DET}$ output is logic high. The $C_D$ filter capacitor is calculated according to $C_D = T / R_D$ with time constant $T=0.5$ ms. Note that $C_D$ may not be required if $\text{DET}$ is software filtered.

Ground Key Detector

The ground key detector is indicating when the ground key is pressed (active) by putting the output pin $\text{DET}$ to a logical low level when selected. The ground key detector circuit senses the difference in TIPX and RINGX currents.

Should the current difference exceed the threshold value, $\Delta I_{LOn}$, the detector is triggered. As the current difference decreases the detector is reset at current threshold $\Delta I_{LOff}$. $\Delta I_{LOn} > \Delta I_{LOff}$, i.e. the detector has hysteresis. The triggered detector results in a logic low at the $\text{DET}$ output assuming the ground key detector has been selected via the control input. For $\Delta I_{LOn}$ and $\Delta I_{LOff}$ numerical values, please refer to table “Electrical characteristics”.

Ring Trip Detector

The ring trip detector indicates if the line goes off hook while ringing by putting the $\text{DET}$ output to a logical low level. The impedance changes when the telephone goes off hook and the detector detects the change in the line current. The loop current threshold value, $I_{LTh}$, at which the ring trip detector changes state is programmable by selecting the value of resistor $R_{DR}$. $R_{DR}$ connects between pin RDR and VEE.

Figure 15 shows a block diagram of the ring trip detector. The two-wire interface produces a current flowing out of the pin RDR:

$$I_{RDR} = \frac{|I_{LTIPX} - I_{LRINGX}|}{600} = I_L / 300$$

where $I_{LTIPX}$ and $I_{LRINGX}$ are currents flowing into the TIPX and RINGX terminals and $I_L$ is the loop current. The voltage generated by $I_{RDR}$ across the programming resistor $R_{DR}$ is compared to an internal reference by a comparator. When the loop current exceeds the detector threshold $I_{LTh}$, then the $\text{DET}$
output is logic low. The programming resistor, \( R_{DR} \), can be calculated for a desired \( I_{LTh} \) from:

\[
R_{DR} = \frac{360}{I_{LTh}}
\]

\( R_{DR} \) is in kΩ for \( I_{LTh} \) in mA. When the loop current is less than \( I_{LTh} \), then the DET output is logic high.

For calculation of the loop current during ringing see section "PBL38710/1 Power Dissipation".

The \( C_{DR} \) filter capacitor is calculated according to \( C_{DR} = \frac{T}{R_{DR}} \) with time constant \( T=0.5 \) ms. Note that \( C_{DR} \) may not be required if DET is software filtered. See figure 16 for the behavior of the states at the DET pin and voltage at the RDR pin.

Control Inputs

The PBL 38710/1 SLICs have four TTL compatible digital control inputs HB, E1, C2 and C1.

A decoder in the SLIC interprets the control input condition and sets up the commanded operating state.

Open Circuit State (C2,C1 = 0.0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C2,C1 = 0.1)

To accomplish a high voltage ring signal the battery feed uses the high voltage, \( V_{Bat} \), when the ringing state is chosen. The SLIC will automatically (without any influence of input HB) switch to the high voltage. A low voltage ring signal at pin VR will be amplified and is transferred to the subscriber as a balanced ring signal. For additional information about the ring signal; see the Ring Voltage section. The ring trip detector is indicating off hook with a logic low level at the detector output.

Active State (C2,C1 = 1.0)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. Both the loop current and the ground key detectors are activated. Input E1 control the selection of one of these detectors to be gated to the DET output.

Stand-by State (C2,C1 = 1.1)

Signal transmission is inhibited. In the Stand-by State the line drive amplifiers are disconnected. The loop feed is converted to resistive form.

The battery switch input signal HB controls which battery that is being used for battery feed.

Both the loop and ground key detectors are activated in this operating state. Input E1 control the selection of one of these detectors to be gated to the DET output.

Enable Input (E1)

The TTL compatible input E1 controls the function of the DET output in the active and stand-by states. In open circuit and ringing state the detector to be gated to the DET is automatically chosen by the SLIC when one of these states is selected by input signals C1 and C2.

Table 1 summarizes the above description of the control inputs.

<table>
<thead>
<tr>
<th>Note 1</th>
<th>SLIC operating state</th>
<th>DET output</th>
<th>Battery Feed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X X 0 0</td>
<td>Open circuit</td>
<td>Logic level high</td>
</tr>
<tr>
<td>2</td>
<td>X X 0 1</td>
<td>Ringing</td>
<td>Ring trip status</td>
</tr>
<tr>
<td>3</td>
<td>X 0 1 0</td>
<td>Active</td>
<td>Ground key status</td>
</tr>
<tr>
<td>4</td>
<td>X 1 1 0</td>
<td>Active</td>
<td>Loop current status</td>
</tr>
<tr>
<td>5</td>
<td>0 0 1 1</td>
<td>Stand-by</td>
<td>Ground key status</td>
</tr>
<tr>
<td>6</td>
<td>0 1 1 1</td>
<td>Stand-by</td>
<td>Loop current status</td>
</tr>
<tr>
<td>7</td>
<td>1 0 1 1</td>
<td>Stand-by</td>
<td>Ground key status</td>
</tr>
<tr>
<td>8</td>
<td>1 1 1 1</td>
<td>Stand-by</td>
<td>Loop current status</td>
</tr>
</tbody>
</table>

Table 1. SLIC operating states

Notes

1. Input C1 and C2 selects SLIC operating state, input E1 selects detector (except in open circuit- and ringing state) and input HB selects the battery to be used for battery feed in stand-by state. X symbolises “don’t care”.
2. In the open circuit state the SLIC present a high impedance to the line and no battery is used for battery feed.
3. In stand-by state input HB must be set to select between \( V_{Bat2} \) and \( V_{Bat} \). In the other states the SLIC automatically selects the appropriate battery. If \( |V_{Bat}| > |V_{Bat2}| \)
Ring Voltage

First we define: Crest factor = \frac{\hat{V}}{V_{\text{rms}}}

Table 2 and 3 define the voltage over the bell under different conditions. The bell is modelled according to the USREN (Ringing Equivalence Number) standard. 1 USREN = 6930Ω ± 8 μF @ 20 Hz, so one bell has the impedance 7 kΩ at 20 Hz. 5REN is equal to five 1REN loads in parallel, 1386 Ω ± 40μF is approx. 1.4 kΩ at 20 Hz.

In Table 3 the required \( V_{\text{Bat}} \) to achieve a specific voltage over the bell (40 or 50 V) is presented, the load is fixed at 3 or 5REN with 100 Ω wire resistance. The high voltage ring signal from the SLIC will be balanced about \( V_{\text{Bat}}/2 \).

Overvoltage Protection

The PBL 387 10/1 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC.

Secondary Protection

The circuit shown in figure 12 utilizes series resistors together with a programmable overvoltage protector (e.g. Power Innovations TISP PBL2), serving as a secondary protection. The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage, \( V_g \)). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, \( C_{\text{GG}} \), is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. \( C_{\text{GG}} \) shall be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the \( V_{\text{Bat}} \) supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors \( R_f \) serve the dual purposes of being non-destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross.

Note that it is important to always use PTC’s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

Power-up Sequence

The voltage at pin \( V_{\text{Bat}} \) sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The optimal power up sequence is ground, \( V_{\text{Bat}} \) and then other supplies and signal leads.

However, \( V_{\text{CC}} \) may be connected before \( V_{\text{Bat}} \) and if the \( V_{\text{Bat}} \) supply voltage should be absent, a diod connected between \( V_{\text{EE}} \) and pin \( V_{\text{Bat}} \), see diod \( D_{BE} \) in figure 12, ensures the presence of the most negative supply voltage at the \( V_{\text{Bat}} \) pin. The \( V_{\text{Bat}} \) and \( V_{\text{Bat}2} \) pins should not be applied at a faster rate than corresponds to the time constant formed by 5.1 Ω resistors, \( R_{\text{Bat}} \) and \( R_{\text{ Bat2}} \) in figure 12, in series with the \( V_{\text{Bat}} \) and the \( V_{\text{Bat}2} \) pins and 0.47 mF capacitors, \( C_{\text{ Bat}} \) and \( C_{\text{ Bat2}} \) in figure 12, from the \( V_{\text{Bat}} \) and \( V_{\text{Bat}2} \) pins to ground. These RC networks may be shared with several SLICs.

Printed Circuit Board Layout

Care in PCB layout is essential for proper function. The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN pin. Ground plane surrounding the RSN pin is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) on the PCB in one point.
Figure 17. Loop current as a function of loop resistance.

Figure 18. Tip-ring voltage as a function of loop resistance.

Figure 19. Loop current as a function of loop resistance.

Figure 20. Tip-ring voltage as a function of loop resistance.
Figure 21. Overload level, $V_{TRO}$ as a function of $V_{Margin}$.

Figure 22. Loop resistance at $I_L = 18$ mA as a function of $V_{Margin}$ at open loop.

Figure 23. Power dissipation.
**Ordering Information**

<table>
<thead>
<tr>
<th>Package</th>
<th>Temp. Range</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 pin PLCC Tube</td>
<td>-40° to +85°C</td>
<td>PBL 387 10/1QNS</td>
</tr>
<tr>
<td>28 pin PLCC Tape &amp; Reel</td>
<td>-40° to +85°C</td>
<td>PBL 387 10/1QNT</td>
</tr>
</tbody>
</table>

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