MB86934

930 Series 32–BIT RISC EMBEDDED PROCESSOR

June 1996

FEATURES

- 50 MHz operating frequency, 40 MHz operating frequency when FIFO is used
- SPARC® high performance RISC architecture
- High Performance SPARC FPU, ANSI/IEEE 754 compatible
- 8 Kbytes 2-way set associative instruction cache
- 2 Kbytes 2-way set associative data cache
- High Bandwidth synchronous DRAM (SDRAM) interface
- 6 on-chip FIFOs which can be used as source and destination for FPU operations
- 2 channel DMA controller capable of transferring data to and from the FIFOs
- Support for burst mode cache fills
- Flexible locking mechanism for data and instruction cache entries
- Harvard-style separate instruction and data buses on-chip
- 8 window, 136 word register file
- Fast interrupt response time
- 247 address spaces, 4 Gbyte each
- Bus Interface Unit runs at half the 50/40 MHz processor speed
- Buffered writes and instruction pre-fetching
- Fast page-mode DRAM support
- Support for execution out of 8, 16, or 32-bit wide boot memory
- Parity generation and checking
- Programmable address decoder and wait-state generator
- 16-bit auto reload timer
- JTAG test interface
- Emulator support hardware
- Single vector trapping
- Power down modes
- 0.5 micron gate, 3 level metal CMOS technology, 3.3V internal and 3.3V/5V I/O

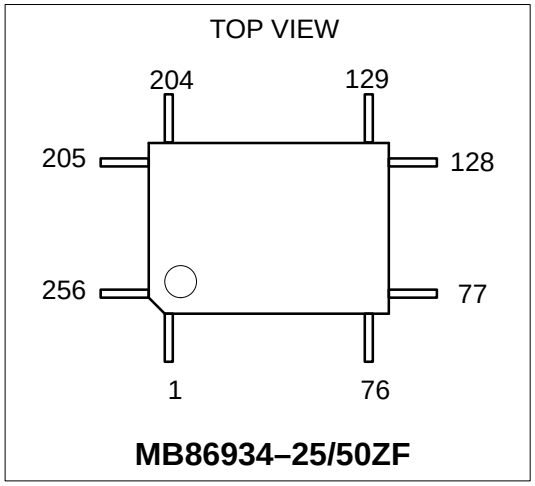
GENERAL DISCUSSION

The MB86934 is the fifth of the 930 series of RISC processors which offers high performance and high integration for a wide range of embedded applications. The processor is based on the SPARC architecture and is upward code compatible with previous implementations. At 50 MHz, the processor executes with 50 MIPs peak and 46 MIPs sustained performance.

The FPU implemented on the MB86934 is compatible with ANSI/IEEE-754-1985. It is also fully compatible with Ver. 8 SPARC FPU. To improve the performance of the chip, the MB86934 supports “Enhanced Floating Point Operations”. These operations can have their operands in 6 on-chip FIFOs or the floating point registers. The on-chip FIFOs decouple the FPU from external memory latency. Using the Enhanced Floating Point operations, the FIFOs and SDRAMs the MB86934 can perform single precision floating point operations at the rate of 40 MFLOPS, at 40 MHz.

The SDRAM interface allows the MB86934 to interface to SDRAMs, which can provide data at the peak rate of 400 MBytes/sec.

PIN CONFIGURATION



MB86934–25/50ZF

PIN CONFIGURATIONS

PIN NO.	PIN NAME TYPE	PIN NO.	PIN NAME TYPE	PIN NO.	PIN NAME TYPE	PIN NO.	PIN NAME TYPE
1	D<40>	55	IRL<1>	109	VSS	163	VSS
2	D<41>	56	IRL<2>	110	IO_VDD	164	IO_VDD
3	VSS	57	IRL<3>	111	VSS	165	–SCS0
4	VDD	58	TDO	112	VDD	166	–SCS1
5	VSS	59	TRST	113	ADR<18>	167	–SCS2
6	D<42>	60	TDI	114	ADR<19>	168	–SCS3
7	D<43>	61	TMS	115	ADR<20>	169	–SCAS
8	IO_VDD	62	TCK	116	ADR<21>	170	VSS
9	VSS	63	EMU_SD<3>	117	ADR<22>	171	–SRAS
10	D<44>	64	EMU_SD<2>	118	ADR<23>	172	–OE
11	D<45>	65	EMU_SD<1>	119	VSS	173	–NVWE
12	D<46>	66	EMU_SD<0>	120	IO_VDD	174	–ERROR
13	D<47>	67	EMU_VDD	121	ADR<24>	175	–LOCK
14	VSS	68	VSS	122	ADR<25>	176	–BGRNT
15	VDD	69	EMU_D<3>	123	ADR<26>	177	–PBREQ
16	D<48>	70	EMU_D<2>	124	ADR<27>	178	VSS
17	D<49>	71	EMU_D<1>	125	ADR<28>	179	IO_VDD
18	D<50>	72	EMU_D<0>	126	ADR<29>	180	–BMREQ
19	IO_VDD	73	–EMU_ENB	127	ADR<30>	181	VSS
20	VSS	74	–EMU_BRK	128	VSS	182	VDD
21	D<51>	75	VDD	129	VDD	183	RD/–WR
22	D<52>	76	VSS	130	ADR<31>	184	–AS
23	D<53>	77	–DACK0	131	ASI<0>	185	VSS
24	VSS	78	–EOP0	132	ASI<1>	186	VDD
25	VDD	79	–DREQ0	133	VSS	187	–READYOUT
26	D<54>	80	–DACK1	134	IO_VDD	188	–READY
27	D<55>	81	VSS	135	ASI<2>	189	–MEXC
28	D<56>	82	IO_VDD	136	ASI<3>	190	–BMACK
29	D<57>	83	–EOP1	137	–BE3	191	VSS
30	IO_VDD	84	–DREQ1	138	–BE2	192	VDD
31	VSS	85	ADR<2>	139	–BE1	193	–BREQ
32	D<58>	86	ADR<3>	140	–BE0	194	–RESET
33	D<59>	87	ADR<4>	141	–SAME_PAGE	195	–PDRESET
34	D<60>	88	ADR<5>	142	–CS0	196	D<0>
35	D<61>	89	VSS	143	–CS1	197	D<1>
36	D<62>	90	VDD	144	–CS2	198	D<2>
37	VSS	91	VSS	145	VSS	199	VSS
38	VDD	92	IO_VDD	146	IO_VDD	200	IO_VDD
39	D<63>	93	ADR<6>	147	–CS3	201	D<3>
40	PARITY<0>	94	ADR<7>	148	VSS	202	D<4>
41	IO_VDD	95	ADR<8>	149	VDD	203	D<5>
42	VSS	96	ADR<9>	150	–CS4	204	VDD
43	PARITY<1 >	97	ADR<10>	151	XTAL2	205	VSS
44	PARITY<2>	98	VSS	152	XTAL1 / CLKIN	206	D<6>
45	PARITY<3>	99	VDD	153	CLKOUT1	207	D<7>
46	–TIMER_OVF	100	ADR<11>	154	CLKOUT2	208	D<8>
47	BIUCLOCK	101	VSS	155	A_VSS	209	D<9>
48	–CLKDBL	102	IO_VDD	156	A_VDD	210	VDD
49	CLK_ECB	103	ADR<12>	157	VSS	211	VSS
50	–BMODE8	104	ADR<13>	158	VDD	212	D<10>
51	–BMODE16	105	ADR<14>	159	SCKE	213	VSS
52	IRL<0>	106	ADR<15>	160	–SWE	214	IO_VDD
53	VSS	107	ADR<16>	161	SDQM0	215	D<11>
54	VDD	108	ADR<17>	162	SDQM1	216	D<12>

PIN CONFIGURATIONS

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
217	D<13>		227	D<19>		237	VSS		247	D<33>	
218	D<14>		228	D<20>		238	IO_VDD		248	D<34>	
219	D<15>		229	D<21>		239	D<27>		249	VSS	
220	VDD		230	D<22>		240	D<28>		250	IO_VDD	
221	VSS		231	D<23>		241	D<29>		251	D<35>	
222	D<16>		232	VDD		242	D<30>		252	D<36>	
223	D<17>		233	VSS		243	D<31>		253	D<37>	
224	D<18>		234	D<24>		244	D<32>		254	D<38>	
225	VSS		235	D<25>		243	VDD		255	D<39>	
226	IO_VDD		236	D<26>		246	VSS		256	IO_VDD	

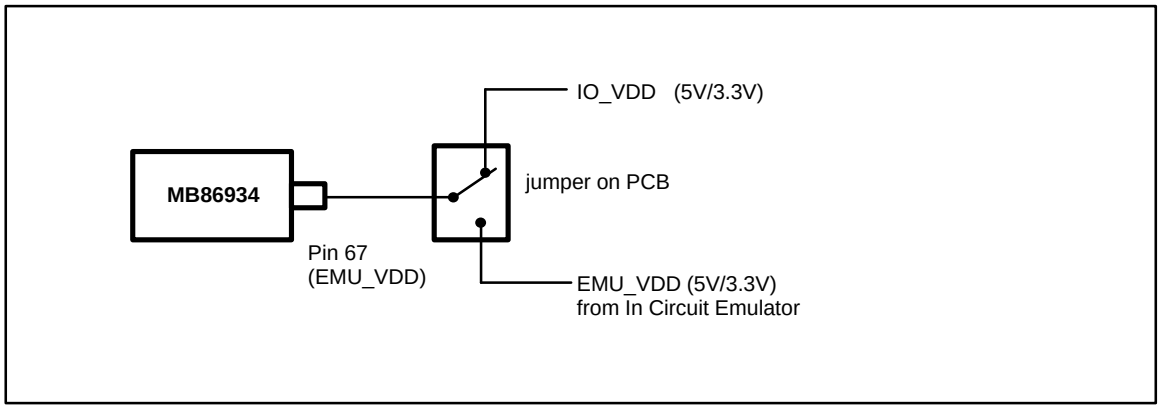
NOTE: ① PIN47(BIUCLOCK) must be tied to I/O_VDD.

NOTE: ② PIN49 (CLK_ECB) must be tied to VSS.

NOTE: ③ PIN155 (A_VSS) and PIN156 (A_VDD) must be very clean.
If necessary, use LC type Low–pass Filter.

NOTE: ④ PIN67 (EMU_VDD) must be tied to IO_VDD when in circuit emulator is not used as shown below.

< EXAMPLE >



ORDERING CODE

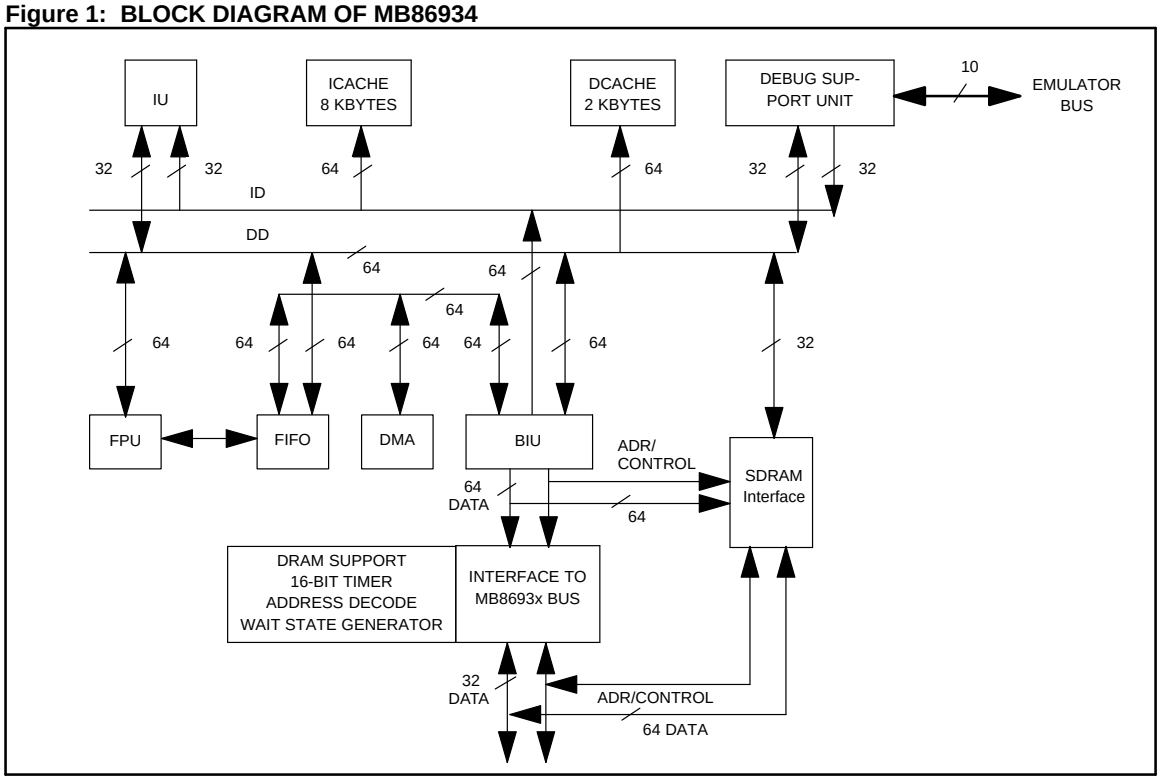
Clock Frequency (MHz)	Ordering Code	Package Type
25/50	MB86934–25/50ZFVES	256–Pin CQFP

On–chip data and instruction caches are included to help decouple the processor from external memory latency. Separate on-chip instruction and data paths provide a high bandwidth interface between the IU and caches. An on-chip 2-channel DMA controller makes use of the processor bus even while the integer unit or floating point unit are executing out of cache. Included to maximize the performance of the system with minimum glue logic, are chip select outputs, programmable wait state generation, built-in support for connection to page-mode DRAM and support for booting from 8 and 16-bit memory. See MB86934 block diagram.

Support for debug and diagnostic tools has been included on-chip and allows for direct connection to hardware emulators and improves debug capability when using ROM based monitors.

These features combine to give the MB86934 superior speed, flexibility and efficiency to make it the ideal choice for a wide variety of low cost, high performance embedded systems.

Figure 1: BLOCK DIAGRAM OF MB86934



SIGNAL DESCRIPTIONS[1]

SYMBOL	TYPE	DESCRIPTION
–RESET	I	**SYSTEM RESET:** Asserting reset for at least 4 processor cycles after the clock has stabilized, causes the MB86934 to be initialized.
CLK_IN (XTAL1)	I	**EXTERNAL OSCILLATOR:** The frequency of the CLK_IN input determines the frequency of operation of the bus. The internal frequency of operation of the part is a function of the frequency of the CLK_IN signal and the –CLKDBL signal.
XTAL2, CLKOUT1, CLKOUT2	O	**CLOCK OUTPUTS:** These signals are used for chip testing.
–LOCK	O S(L) G(Z) I(1)	**BUS LOCK:** This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction for example requires contiguous bus transactions which cause the assertion of the bus lock signal. The bus may not be granted to another bus owner as long as –LOCK is active. –LOCK is asserted with the assertion of AS as remains active until –READY is asserted at the end of the locked transaction.
–BREQ	I S(L)	**BUS REQUEST:** Asserted by another device on the bus to indicate that it wants ownership of the bus. The request must be answered with a bus grant (–BGRNT) from the MB86934 before the device can proceed by driving the bus. Once the bus has been granted, the device has ownership of the bus until it de-asserts –BREQ. The user should ensure that devices on the bus cannot monopolize the bus to the exclusion of the CPU. Inputs to –BREQ while –RESET is active are valid and cause Bus Grant to be asserted.
–BGRNT	O S(L) G(0) I(Q)	**BUS GRANT:** Asserted by the CPU in response to a request from a device wanting ownership of the bus. The CPU grants the bus to other devices only after all transfers for the current transaction are completed. All bus drivers are three-stated with the assertion of the bus grant signal.
–ERROR	O S(L) G(Q) I(Q)	**ERROR SIGNAL:** Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the the tt value in the TBR, enters into an error state and asserts the –ERROR signal. The system can monitor the –ERROR pin and initiate a reset under the error condition. This pin is high on reset.
–MEXC	I S(L)	**MEMORY EXCEPTION:** Asserted by the memory system to indicate a memory error on either a data or instruction access. Assertion of this signal initiates wither a data or instruction access exception trap in the IU. The current bus access is invalidated by asserting the –MEXC in the same cycle as the –READY signal. The IU ignores the contents of the data bus in cycles where –MEXC is asserted.
IRL <3:0>	I A(L)	**INTERRUPT REQUEST BUS:** The value on these pins defines the external interrupt level. IRL <3:0>=1111 forces a non-maskable interrupt. IRL value of 0000 indicates no pending interrupts. Al l other values indicate maskable interrupts as enabled in the PIL field of the processor status register (PSR). Interrupts should be latched and prioritized by external logic and should be held pending until acknowledged by the processor.

SIGNAL DESCRIPTIONS[1] (Continued)

<table>
<tr><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>–TIMER_OVF</td><td>O
S(L)
G(Q)
I(Q)</td><td>TIMER UNDERFLOW: Asserted by the processor to indicate that the internal 16-bit timer has underflowed. This signal can be used to initiate a DRAM refresh cycle of a one cycle periodic waveform. On reset, the timer is turned off and –TIMER_OVF is high.</td></tr>
<tr><td>–SAME_PAGE</td><td>O
S(L)
G(1)
I(1)</td><td>SAME-PAGE DETECT: The –SAME_PAGE signal is used to take advantage of fast consecutive accesses within the same page for Fast Page Mode DRAMs. This signal is an output which is asserted when the current access in the region defined by chip select 4 is in the same page as the previous access to chip select 4. The page size is specified by writing it the SAME_PAGE MASK register.</td></tr>
<tr><td>–CS0, –CS1,
–CS2, –CS3,
–CS4</td><td>O
S(L)
G(1)
I(1)</td><td>CHIP SELECTS: These outputs are asserted when the value on the bus matches the address range in one of the corresponding ADDRESS RANGE registers. The signals are used to decode the current address into one of five address ranges. Address ranges should not overlap. Each address range has a corresponding wait specifier which is used to automatically assert internal ready after a user defined number of bus clock cycles. This allows a variety of memory and I/O devices with different access times to be connected to the MB86934 without the need for additional logic.</td></tr>
<tr><td>ADR <31:2></td><td>I/O
S(L)
G(Z)
I(1)</td><td>ADDRESS BUS: The 30-bit ADDRESS BUS (A31-A2) is an output which identifies the data or instruction address of a 32-bit word. Reads are always one word in size while byte, half–word, or word transaction sizes for writes is identified by separate byte-enable signals (–BE0-3). The address bus is valid for the duration of the bus transaction. ADR<15:2> are shared by the SDRAM interface.</td></tr>
<tr><td>ASI <3:0></td><td>I/O
S(L)
G(Z)
I(1)</td><td>ADDRESS SPACE IDENTIFIERS: The ADDRESS SPACE IDENTIFIERS are outputs which indicate to which of 256 available spaces the current ADDRESS BUS value corresponds. ASI values are defined as follows:

<table>
<tr><th>ASI</th><th>ADDRESS SPACE</th></tr>
<tr><td>0x1</td><td>Control Register</td></tr>
<tr><td>0x2</td><td>Instruction Cache Lock</td></tr>
<tr><td>0x3</td><td>Data Cache Lock</td></tr>
<tr><td>0x4 - 0x7</td><td>Application Definable</td></tr>
<tr><td>0x8</td><td>User Instruction Space</td></tr>
<tr><td>0x9</td><td>Supervisor Instruction Space</td></tr>
<tr><td>0xA</td><td>User Data Space</td></tr>
<tr><td>0xB</td><td>Supervisor Data Space</td></tr>
<tr><td>0xC</td><td>Instruction Cache Tag RAM</td></tr>
<tr><td>0xD</td><td>Instruction Cache Data RAM</td></tr>
<tr><td>0xE</td><td>Data Cache Tag RAM</td></tr>
<tr><td>0xF</td><td>Data Cache Data RAM</td></tr>
<tr><td>0x10 - 0xFC</td><td>Reserved</td></tr>
<tr><td>0xFD - 0xFF</td><td>Reserved for Debug Hardware</td></tr>
</table>

The ASI values specified as “application definable” can be used by supervisor mode instructions such as Load Alternate and Store Alternate. The ASI value is available in the same cycle in which the corresponding address value asserted on the address bus. The ASI pins are valid for the duration of the bus transaction. ASI values 0x8, 0x9, 0xA, and 0xB are cacheable.</td></tr>
</table>

SIGNAL DESCRIPTIONS[1] (Continued)

<table>
<tr><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>–BMODE8</td><td>I
S(L)</td><td>8-BIT BOOT MODE: This signal is sampled during reset and causes read accesses, memory mapped to –CS0, to assume 8-bit memory. The MB86934 generates four sequential fetches to assemble a complete instruction or data word before continuing. Bytes are fetched in sequence (0,1,2,3) as encoded by –BE[2] and –BE[3] (00, 01, 10, 11). Writes to –CS0 are unaffected by boot mode selection and if left unconnected, a weak pull-up on this pin (and –BMODE16 pin) causes the processor to default to 32-bit mode.
Note: BMODE8 and BMODE16 should not be asserted at the same time.</td></tr>
<tr><td>–BMODE16</td><td>I
S(L)</td><td>16-BIT BOOT MODE: This signal is sampled during reset and causes read accesses, memory mapped to –CS0, to assume 16-bit memory. The MB86934 generates two sequential fetches to assemble a complete instruction or data word before continuing. Half words are fetched in sequence (0,1) as encoded by –BE[2]. Writes to –CS0 are unaffected by boot mode selection. If left unconnected, a weak pull-up on this pin (and –BMODE8 pin) causes the processor to default to 32-bit mode.
Note: BMODE8 and BMODE16 should not be asserted at the same time.</td></tr>
<tr><td>–BE3–0</td><td>O
S(L)
G(Z)
I(O)</td><td>BYTES ENABLES : These pins indicate whether the current store transaction is a byte, half-word or word transaction. –BE0-3 signals are availa ble in the same cycle in which the corresponding address value is asserted on the address bus and is valid for the duration of the bus transaction. This bus should be used only to qualify store transactions. For load transactions all sub-word requests are read (and replaced in the cache) as words and then the appropriate byte or half-word is extracted by the integer unit
Possible values for –BE3-0 are a follows:
<table>
<tr><th></th><th>Byte0
31 24</th><th>Byte1
23 16</th><th>Byte2
15 8</th><th>Byte3
7 0</th></tr>
<tr><td>Byte Writes</td><td>1 1 1 0</td><td>1 1 0 1</td><td>1 0 1 1</td><td>0 1 1 1</td></tr>
<tr><td>Half-Word Writes</td><td colspan="2">1 1 0 0</td><td colspan="2">0 0 1 1</td></tr>
<tr><td>Word Writes</td><td colspan="4">0 0 0 0</td></tr>
</table>
BE<2:3> are also used in 8 and 16-bit ROM accesses as follows:
<table>
<tr><th>Bus Mode</th><th>Byte</th><th>BE<2:3></th></tr>
<tr><td>8-bit</td><td>0
1
2
3</td><td>00
01
10
11</td></tr>
<tr><td>16-bit</td><td>0&1
2&3</td><td>00
10</td></tr>
</table></td></tr>
<tr><td>D <63:0></td><td>I/O
S(L)
G(Z)
I(1)</td><td>DATA BUS: The bus interface has 32 bi-directional data pins D<31:> to transfer data in thirty-two bit quantities. D(31) corresponds to the most significant bit if the least significant byte of the 32-byte word.
In write bus cycles, the point at which data is driven onto the bus depends on the type of the preceding cycle. If the preceding cycle was a write, data is driven in the cycle immediately following the cycle in which –READY was asserted. If the preceding cycle was a read, data is driven one cycle after the cycle in which –READY was asserted to minimize bus contention between the processor and the system.
Pins D<7:0> are used when the 8-bit boot mode is enabled and D<15:0> are used when16-bit mode is enabled.
the SDRAM interface has 64 bidirectional pins D<63:0>. D<63:32> are used exclusively by the SDRAM interface. D<31:0> are shared by the SDRAM interface with the MB8693x bus interface.</td></tr>
</table>

SIGNAL DESCRIPTIONS[1] (Continued)

SYMBOL	TYPE	DESCRIPTION
–AS	I/O S(L) G(Z) I(1)	**ADDRESS STROBE:** A control signal asserted by the MB86934 or other bus master to indicate the start of a new bus transaction. A bus transaction begins with the assertion of –AS and ends with the assertion of –READY. –AS remains asserted for 1 clock cycle. During cycles in which neither the processor nor another bus master is driving the bus the bus is idle, and –AS remains de-asserted.
RD/–WR	I/O S(L) G(Z) I(1)	**READ/WRITE TRANSACTION:** This signal specifies whether the current bus transaction is a read or a write operation. When –AS is asserted and RD/–WR is low, then the current transaction is a write. With –AS asserted and RD/–WR high, the current transaction is a read, RD/–WR remains active for the duration of the bus transaction and is de-asserted with the assertion of –READY.
–READY	I S(L)	**READY:** This is a control signal asserted by the external memory system to indicate that the current bus transaction is being completed and that it is ready to start with the next bus transaction in the following cycle. In case of a fetch from memory, the processor will strobe the value on the data bus at the rising edge CLK_IN following the assertion of –READY. For the case of a write, the memory system will assert –READY when the appropriate access time has been met. In most cases, no additional logic is required to generate the –READY signal. On-chip circuitry can be programmed to assert –READY internally based on the address of the current transaction. The external system can override the internal ready generator to terminate the current bus cycle early. Up to 6 address ranges each with different transaction times can be programmed.
–DREQ0-1	I A(L)	**DMA REQUEST:** Indicates that an external device is requesting a DMA transfer. This signal is edge sensitive for single transfers and level sensitive for demand transfer. –DREQ0 corresponds to DMA channel 0, while –DREQ1 corresponds to DMA channel 1.
–DACK0-1	O S(L)	**DMA ACKNOWLEDGE:** This is asserted when an external device asserts –DREQ and the processor accesses the external device. –DACK1 corresponds to DMA channel 0, while –DACK1 corresponds to DMA channel 1.
–EOP0-1	I/O S(L)	**END OF PROCESS:** The signal is asserted by the external device when it wants to terminate a DMA transfer. Alternately, the processor drives this signal when the byte count reaches zero. –EOP0 corresponds to DMA channel 0, while –EOP1 corresponds to DMA channel 1. A pull-up holds –EOP0-1 high when it is not being driven.
–PBREQ	O S(L)	**PROCESSOR BUS REQUEST:** This signal is asserted by the processor to indicate to an external bus arbiter that it needs to regain control of the bus. This provides a hand shake between the arbiter and the processor to allow the bus to be allocated based on demand.
–BMREQ	O S(L)	**BURST MODE REQUEST:** This signal is asserted by the processor to indicate to an external system that the processor's burst mode is enabled and the current transaction can be a burst. If the external system supports burst mode, it asserts –BMACK concurrently with –RDY to begin the burst mode transfer.
–BMACK	I S(L)	**BURST MODE ACKNOWLEDGE:** This signal is asserted by the system to indicate that it can support burst mode for the address currently on the bus. The system asserts –BMACK in response to the processor asserting –BMREQ.
CLK_ECB	I	**EXTERNAL CLOCK BYPASS:** This signal is used for chip testing and should be tied low during normal operation.
–CLKDBL	I	**CLOCK DOUBLER:** Tying this signal low causes the internal logic to run at twice the frequency of the clock input.

SIGNAL DESCRIPTIONS[1] (Continued)

SYMBOL	TYPE	DESCRIPTION
PARITY <3:0>	I/O S(L)	**PARITY*:** When enabled this signal provides even or odd parity checking for the data bus. NOTE: PARITY3 is for Byte 0 / Half–Word 0. (See Table below ***)
–SWE	OS(L)	**SDRAM Write Enable:** This signal should be tied to the –WE input of SDRAM.
–SRAS	OS(L)	**SDRAM Row Address Strobe:** This signal should be tied to the –RAS input of SDRAM.
–SCAS	OS(L)	**SDRAM Column Address Strobe:** This signal should be tied to the –CAS input of SDRAM.
–SCS <3:0>	OS(L)	**SDRAM Chip Select:** Enables all command inputs, –RAS, –CAS, and –WE to SDRAM.
SCKE	OS(L)	**SDRAM Clock Enable:** This is an active high clock enable signal for SDRAM.
SDQM <1:0>	OS(L)	**SDRAM INPUT MASK/OUTPUT ENABLE:** SDQM<0> and SDQM<1> correspond to D<63:32>and <31:0> respectively.
–NVWE	OS(L)	**WRITE ENABLE FOR NON-VOLATILE MEMORY:** This signal is asserted one cycle after –AS and stays asserted till one cycle before the end of the transaction for a write operation. The signal is generated only when internal wait state generation is enabled for the current access.
–OE	O S(L)	**OUTPUT ENABLE:** This signal is asserted one cycle after –AS and stays asserted till the last cycle of a read operation. This signal is generated when internal wait state generation is enabled for the current access.
–READYOUT	OS(L)	Ready Out for external Bus Masters using Internal Ready Generation.
–PDRESET	I S(L)	Power Down Reset is asserted by the external system to get the part out of powerdown mode.
BIUCLOCK	I	This signal is reserved for future use and should be tied high.
EMU_SD <3:0>	I/O	**EMULATOR STATUS/DATA BITS:** Bi-directional pins used by a hardware emulator to control and monitor MB86934 execution. These pins should be left unconnected.
EMU_D <3:0>	I/O	**EMULATOR DATA BITS:** Bi-directional pins used by a hardware emulator to control and monitor MB86934 execution. These pins should be left unconnected.
–EMU_BRK	I	**EMULATOR BREAK REQUEST LINE:** Input used by a hardware emulator to request a trap when emulation is enabled. This pin should be unconnected.
–EMU_ENB	I/O	**EMULATOR ENABLE:** Tied low while the MB86934 is being reset to enable hardware emulator mode on the chip. This pin should be left unconnected.
TCK	I	**TEST CLOCK:** JTAG compatible test clock input.
TMS	I	**TEST MODE:** JTAG compatible test mode select pin. Test is enabled when–TMS is low.
TDI	I	**TEST DATA IN:** JTAG compatible test data input.
TDO	O	**TEST DATA OUT:** JTAG compatible test data output.
–TRST	I	**TEST RESET:** Asynchronous rest for JTAG logic. If not using JTAG, this signal must be pulled low.

*	PARITY3	PARITY2	PARITY1	PARITY0
BIU	D<31: 24>	D<23:16>	D<15: 8>	D<7: 0>
SDRAM	D <63: 48>	D <47: 32>	D <31: 16>	D <15: 0>

1. In the following description, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

Notes:
- I =Input Only Pin
- O =Output Only Pin
- I/O =Either Input or Output Pin
- – =Pins "must be" connected as described
- A(L) =Asynchronous: Inputs may be asynchronous to CLKOUT.
- S(L) =Synchronous: Inputs must meet setup and hold times relative to CLK_IN Outputs are Synchronous to CLK_IN

G(…)=While the bus is granted to another bus master (–BGRNT=asserted), the pin is
- G(1) is driven to V_{CC}
- G(0) is driven to V_{SS}
- G(Z) floats
- G(Q) is a valid output

I (…) =While the bus is between bus cycles (or being reset) and is not granted to another bus master, the pin is
- I (1) is driven to V_{CC}
- I (0) is driven to V_{SS}
- I (Z) floats
- I (Q) is a valid output

OVERVIEW

The Fujitsu MB86934 is a high performance, 32-bit RISC processor which executes at 50 MIPS peak and 46 MIPs sustained performance with 50 MHz clock frequency. It has a floating point Unit that performs single precision multiply and single precision adds at the rate of 1 per cycle. Like its predecessors, the MB86934 is based on the SPARC architecture and is upward code compatible with previous implementations. The MB86934 has been developed specifically with the needs of embedded applications in mind and offers high performance and high integration for these applications.

The MB86934 instruction set is streamlined and hardwired for fast execution with most instructions executing in a single cycle. The Integer Unit (IU) features a 5-stage pipeline which has been designed to handle data interlocks, has an optimized branch handler for efficient control transfers, and a bus interface to handle single cycle bus accesses to on-chip memory.

An internal register file consisting of 136 registers organized into eight overlapping windows speeds interrupt response time and context switches. The register file minimizes accesses to memory during procedure linkages and facilitates passing of parameters and assignment of variables.

On-chip 8 Kbyte instruction and 2 Kbyte data caches have been added to decouple the processor from external memory. These caches have been designed with maximum flexibility in mind and allow entries to be locked to improve overall system performance.

The FPU gets data from a 32 word register file for all standard FPU instructions. The enhanced FPU instructions may get their data from the FIFOs or some of the FPU registers as described later. The FIFOs decouple the FPU from external memory latency.

The SDRAM interface provides a mechanism to easily interface to SDRAMs. These DRAMs are capable of providing data at a peak rate of 400 Mbytes/sec. The DMA and FIFOs coupled with the SDRAM interface provide a cost effective way of providing data to the FPU at very high rates.

Separate 32-bit on-chip instruction and data paths provide a high bandwidth interface between the IU and on-chip cache. These buses support single cycle instruction execution as well as single cycle data transfers with the cache.

The internal data path between the data cache and the FPU is 64-bits wide. This allows the loading of a double precision operand from the cache to the FPU register file in one cycle.

The MB86934 also includes hardware for integer multiply and divide. The hardware support significantly improves the performance of these operations with 32-bit integer multiplies executing in 5 clock cycles, 16-bit integer multiplies in 3 cycles, 8-bit integer multiplies in 2 cycles, and a multiply by zero can complete in a single cycle.

KEY FEATURES

Fast Integer Unit Instruction Execution: Simple functions make up the bulk of instructions in most programs so that execution speed can be greatly improved by designing these instructions to execute in as short a time as possible. The majority of instructions execute in one cycle with only a few of the more complex, such as integer multiply, taking additional cycles.

Fast Floating Point Unit: The high performance FPU implemented on the MB86934 executes all Single/ Double precision operations. The FPU has a three stage pipeline. All single precision operations, except the Divide and Square Root are executed at the rate of one per cycle. Double Precision Add and Subtract are also executed at the rate of one per cycle.

On-chip FIFOs to assist in vector operation: The FPU instructions get their operands from a 32-bit register file. Enhanced FPU instructions get their operands from either the FPU register file or from the 6 FIFOs on-chip. Data can be loaded into the FIFOs or from the FIFOs into memory by the DMA controller. For operations on large arrays of data, the FIFOs and the DMA controller relieve the application program of the task of address generation and moving data to and from memory. This provides a significant improvement in performance for vector operations.

Large Register Set: The large register set for the IU reduces the number of required accesses to data memory. The registers are organized in overlapping groups called register windows which allows registers to be reserved for high priority tasks, such as interrupts, or for recurring requirements such as operating system working registers. The overlapping windows also simplify parameter passing during procedure linkage and reduce code in most programs.

On-Chip Caches: To decouple the speed of the processor from the memory sub-system, data and instructions caches have been added. The caches are organized as two-way set-associative for improved hit rates. In addition, the set-associative caches organization allows entries to be locked, while the rest of the cache performs normally.

Cache Locking: Both data and instruction entries can be locked into their respective caches to ensure deterministic response and highest performance for critical or frequently recurring routines. Maximum flexibility has been designed into the cache to allow all or selected portions to be locked.

Bus Interface: The requirement for glue logic between the MB86934 and the system is minimized by providing

programmable chip selects, programmable wait state circuitry, and support for connection to fast page-mode DRAM. Multiple bus masters are supported through a simple handshake protocol. The MB86934 can boot from either 8, 16 or 32-bit wide memory. For high frequency operation, the bus is capable of running at half the speed of the core.

SDRAM Interface: The Bus interface also provides support to directly connect to high performance SDRAM. The SDRAM interface will support up to four banks of memory. A bank can be 32 or 64 bits wide. The SDRAM controller is designed to interface to 4M (x8), 16M (x4 and x8) and 64M (x8) SDRAMs. The smallest memory size that can be supported is 2Mbytes and the largest memory size can be 512Mbytes.

Table 1. MB86934 Instruction Set

LOGICAL	ARITHMETIC/SHIFT	DATA MOVEMENT	FPU INSTRUCTIONS
CONDITION CODES UNCHANGED AND OR XOR AND NOT OR NOT XNOR **CONDITION CODES SET** AND OR XOR AND NOT OR NOT XNOR	**CONDITION CODES UNCHANGED** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) SCAN SETHI SHIFT LEFT LOGICAL SHIFT RIGHT LOGICAL SHIFT RIGHT ARITHMETIC **CONDITION CODES SET** ADD SUBTRACT MULTIPLY(SIGNED/UNSIGNED) MULTIPLY STEP DIVIDE STEP **EXTENDED AND CONDITION CODES UNCHANGED** ADD SUBTRACT **EXTENDED AND CONDITION CODES SET** ADD SUBTRACT **TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW)** ADD SUBTRACT	**TO USER/SUPERVISOR SPACE SIGNED** LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLE WORD **TO USER SPACE UNSIGNED** LOAD BYTE LOAD HALF-WORD **TO ALTERNATE SPACE SIGNED** LOAD BYTE LOAD HALF-WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF-WORD STORE WORD STORE DOUBLEWORD **TO ALTERNATE SPACE UNSIGNED** LOAD BYTE LOAD HALF-WORD **ATOMIC OPERATION IN USER SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE **ATOMIC OPERATION IN ALTERNATE SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE	**CONVERSION** CONVERT INTEGER TO SINGLE CONVERT INTEGER TO DOUBLE CONVERT SINGLE TO INTEGER CONVERT DOUBLE TO INTEGER CONVERT SINGLE TO DOUBLE CONVERT DOUBLE TO SINGLE **MOVE** MOVE NEGATE ABSOLUTE VALUE **SQUARE ROOT** SQUARE ROOT SINGLE SQUARE ROOT DOUBLE **ADD/SUBTRACT** ADD SINGLE ADD DOUBLE SUBTRACT SINGLE SUBTRACT DOUBLE **MULTIPLY/DIVIDE** MULTIPLY SINGLE MULTIPLY DOUBLE MULTIPLY SINGLE TO DOUBLE DIVIDE SINGLE DIVIDE DOUBLE **FLOATING-POINT COMPARE INSTRUCTIONS** COMPARE SINGLE COMPARE DOUBLE COMPARE SINGLE AND EXCEPTION IF UNORDERED COMPARE DOUBLE AND EXCEPTION IF UNORDERED
CONTROL TRANSFER CONDITIONAL BRANCH CONDITIONAL TRAP CALL RETURN SAVE RESTORE JUMP AND LINK			**BRANCH ON FLOATING-POINT CONDITION CODES** BRANCH ALWAYS BRANCH NEVER BRANCH ON UNORDERED BRANCH ON GREATER BRANCH ON UNORDERED OR GREATER BRANCH ON LESS BRANCH ON UNORDERED OR LESS BRANCH ON LESS OR GREATER BRANCH ON NOT EQUAL BRANCH ON EQUAL BRANCH ON UNORDERED OR EQUAL BRANCH ON GREATER OR EQUAL BRANCH ON UNORDERED OR GREATER OR EQUAL BRANCH ON UNORDERED OR LESS OR EQUAL BRANCH ON LESS OR EQUAL BRANCH ON ORDERED
READ/WRITE CONTROL REGISTER READ PSR WRITE PSR READ TBR WRITE TBR READ WIM WRITE WIM READ Y WRITE Y RDASR WRASR		**ENHANCED FPU INSTRUCTIONS** ALL THE FPU INSTRUCTIONS HAVE CORRESPONDING ENHANCED FPU INSTRUCTIONS	
LOAD/STORE FLOATING-POINT LOAD FLOATING-POINT REGISTER LOAD DOUBLE FLOATING-POINT REGISTER LOAD FLOATING-POINT STATE REGISTER STORE FLOATING-POINT STORE DOUBLE FLOATING-POINT STORE FLOATING-POINT STATE REGISTER STORE DOUBLE FLOATING-POINT DEFERRED TRAP QUEUE			

On-Chip DMA: Two DMA channels support contiguous block and chained block transfers. Byte, half–word, word, and quad-word data types are supported. Either fly-by or flow through addressing modes can be selected.

The DMA controller is also capable of transferring data to and from the FIFOs in the fly-by mode.

Enhanced Instruction Set: The MB86934 incorporates Enhanced Floating-Point instructions which provide a significant improvement in performance for vector operations. It also includes a fast integer multiply instruction which executes in a fast 5, 3 or 2 cycles for 32-bit, 16-bit or 8-bit multiplicands. An integer divide-step instruction cuts divide times by a factor of 10 over previous SPARC implementations. A scan instruction supports a single cycle search for the most significant 1 or 0 in a word.

Power Down Modes

The MB86934 supports multiple power down modes. It provides a mechanism to turn off the clock to various functional units. These can be turned off by the application program if it is not using the particular functional unit.

Test and Debug Interface: The MB86934 supports production test through industry standard JTAG boundary scan. Hardware emulation is supported with on-chip breakpoint and single step logic. A dedicated emulator bus provides a means to trace transactions between the integer unit and on-chip cache.

CPU

The MB86934 core is a high performance fully custom implementation of the SPARC architecture. The core is compact to leave room for peripheral integration and yet is designed in a way to allow the major blocks to be customized for varying application requirements. The core is made up of three functional units: the Instruction block, the Address block and the Execute block. (see Figure 2)

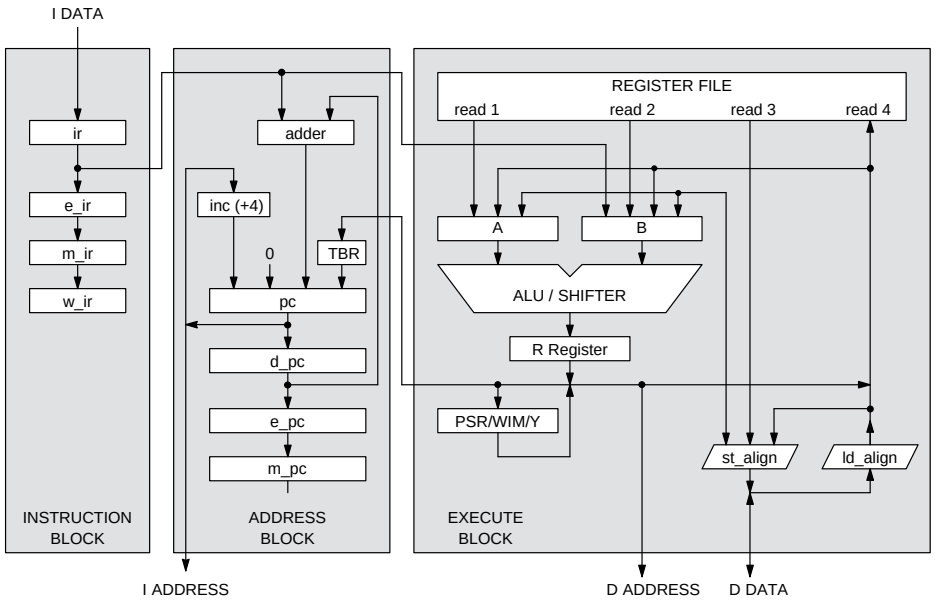


Figure 2. MB86934 Integer Unit Data Path

A five stage instruction pipeline is responsible for decoding all instructions and generating the control signals to the other blocks. The 5-stage pipeline consists of Fetch (F), Decode(D), Execute(E), Memory(M) and Writeback(W). Instruction memory is addressed and returns instructions in the (F) stage, the register file is addressed and returns operands in the (D) stage, the ALU computes results in the (E) stage, external memory is addressed in the (M) stage, and the register file is written back in the (W) stage.

FPU

The high performance FPU implemented on the MB86934 is compatible with the ANSI/IEEE-754-1985 standard. It is fully compatible with SPARC ver. 8 FPU.

The FPU is implemented as a 3 stage pipeline. The FPU executed all Single/Double precision floating point operations. Quad precision floating point operations are not executed by the FPU. All floating point load and stores and Branch on Floating point condition code instructions are executed by the integer unit.

The FPU also executes Enhanced Floating Point Operations. These operations can get their operands from the registers in the FPU register file or the FIFOs (as described in the section on FIFOs). All single and double precision Enhanced Floating Point operations are executed by the FPU. Enhanced Floating-point Load and store operations are not defined.

The performance of the FPU is summarized below:

Floating Point Operation	Throughout (in cycles)	Latency (in cycles)
All comparisons and conversions	1	3
Single Precision ADD/SUB/MUL	1	3
Single Precision DIV/SQRT	13	14
Double Precision ADD/SUB	1	3
Double Precision MUL	4	6
Double Precision DIV/SQRT	28	29

Even though the Floating point queue is 3 deep, whenever a divide or square root enters the queue it is marked as full to prevent any other floating point instructions from entering the queue. This is done to prevent the interrupt latency from being long.

ADDRESS SPACE

The MB86934 offers a large addressing range and allows separate user and supervisor spaces to be defined. In addition to 32 address lines, 4 alternate address space identifiers (ASIs) distinguish between protected and unprotected space. Of the 256 possible ASI values, two define accesses to user data and user instruction space while the remaining ASI values define supervisor space.

Anytime a reset, synchronous trap or asynchronous trap occurs, the processor is placed into the supervisor mode. In this mode, the processor executes instructions and moves data out of supervisor space. While in supervisor mode, the processor also has access to the remaining ASI values. Except for those mentioned and those reserved for control register space, the remaining ASI values can be used to access other alternate data spaces defined by the application.

The distinction of user versus supervisor space allows the hardware to protect against accidental or un-authorized access to system resources. For real time operating system (RTOS) development for example, the separate spaces provide a mechanism for effectively partitioning RTOS space from user space.

REGISTERS

The MB86934 integer unit register set is divided into those used for general purpose functions and those used for control and status.

The 136 general purpose registers are divided into 8 global registers and 8 overlapping blocks or “windows”. Each window contains 24 registers. Of these, 8 are local to the window, 8 “out” registers overlap with the next window and 8 “in” registers overlap with the previous window (see Figure 2).

This organization makes it easy to pass parameters to subroutines. Parameters that are to be passed along are written to the “out” registers and the subsequent procedure call decrements the window pointer to make a new set of registers available. The passed parameters are now available to the subroutine in the current window’s “in” registers.

Register windows improve performance in embedded applications because they function as local variable caches which retain either interrupt, subroutine, context or operating system variables with no additional overhead. In addition, code can be reduced by exploiting the efficient execution of procedure linkage by preventing in-lining compiler optimizations.

The registers that make up the register file each have three read-only and one write-only port. The use of a four port register file allows even store instructions, which may require that three operands be read out of the register file, to proceed at one instruction per cycle.

The control and status registers include those defined by the SPARC architecture (See Table 2) and those

mapped into alternate address space to control peripheral functions (See Table 3).

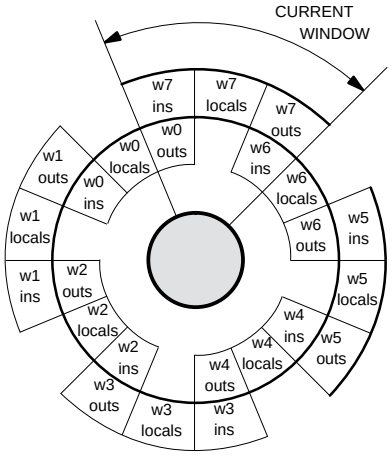


Figure 3. General Purpose Register Organization

INSTRUCTION SET

The MB86934 is upward code compatible with other SPARC processors. Additional instructions, previously not directly supported, have been added to improve performance in embedded applications. Enhanced Floating-point instructions, integer multiply, integer divide step, and scan for first changed bit have been added to the already powerful SPARC instruction set. See Table 1 for a list of supported instructions.

INTERRUPTS

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86934 implementation has been tailored to insure not only low average latency but low maximum latency as well.

Interrupt response time is made up of the sum of the times it takes the processor to finish its current task after recognizing an interrupt, and the time it takes to begin executing interrupt service routine instructions. The MB86934 implements numerous features to minimize both factors.

To minimize the time it takes to finish the current task, the MB86934 is designed so that tasks can either be interrupted or completed in a minimum of cycles. Implementation details that accomplish this aim include cache line misses that can be filled one word at a time through a pre-fetch buffer, integer divide that is interruptible through the use of a divide step instruction, fast multiply and a 1 word write buffer to limit pending bus transactions.

To minimize the time required to start executing the interrupt service routine the processor switches to a new register window when an interrupt is detected. This feature allows the service routine to be executed without first requiring that the current registers be saved. The user can also elect to lock the service routine into the cache. This makes the routine available for immediate access. The on-chip data cache can also serve the service routine as a fast local stack for minimum delay in accessing routine variables.

The MB86934 provides for up to 15 different interrupt levels. The highest interrupt level is non-maskable.

CACHE

The MB86934 has separate on-chip data and instruction caches. This allows the user to build a high performance system without incurring the cost of requiring fast external memory and the associated control logic. The caches are physically mapped.

The instruction cache is organized as two banks of one hundred twenty-eight 32-byte lines (See Figure 5). The data cache is organized as two banks of sixty-four 16-byte lines (See Figure 4).

The lines are organized as two-way set-associative for good performance even when cache locking is in effect. Lines are divided into sub-blocks each four bytes wide. On a cache miss, the caches are updated either 1 word (4 bytes) at a time, or 4 words at a time using the processor's burst mode feature. Single word updates minimize interrupt latency associated with long cache line replacements, while 4 word burst refills maximize the use of available bus bandwidth. An instruction pre-fetch buffer fetches the next sequential instruction anticipating that it will be needed to fill the next instruction cache miss.

The caches can be used in either normal or one of two lock modes. In normal mode, the caches use an LRU (least recently used) algorithm to replace one of the two appropriate entries. Alternately, the two locking modes allow the entire cache or just selected entries to be locked. The lock modes allow time critical routines to be locked in cache.

Global locking allows the entire content of either the instruction or data cache to be frozen. Two control bits in the cache control register enable or disable locking for either cache. With the entire cache locked, no valid entry can be replaced. To insure best possible performance however, invalid entries will be updated if they are accessed. This is done automatically and incurs no time penalty.

Local cache locking makes it possible to dynamically lock selected instructions or data entries into the appropriate cache. This feature gives the flexibility, for

example, to assure deterministic response for certain critical interrupt routines by locking the routine's code into the cache. Entries can also be locked where it is desirable to give performance priority to certain often used routines which might otherwise be removed from cache. The 2-way set-associativity allows the cache to perform effectively even with some locked entries.

In local lock mode, each entry can either be locked individually by software or automatically with hardware assist. For individual locking, software writes the lock bit in the appropriate cache tag line. For automatic locking, a bit in each cache control register enables or disables the feature. The enable bit is set at the beginning of a routine for which the entries are to be locked. This causes the location of any cache access occurring while the bit is enabled to be locked into the cache. In addition to requiring just one initial cycle to enable, automatic entry locking incurs no overhead while in effect. Locked locations can be cleared with a single write to a control register.

In unlocked operation, the data cache uses a write-through update policy and allocates a cache entry only on a load. Writes are buffered so that the processor can continue executing while data is written back to memory. In contrast, writes to locked data cache locations are not written through to main memory. Besides reducing external bus activity, this design supports configuring a portion of data cache as on-chip RAM which does not map to external memory.

The data and instruction caches are designed to be accessed independently over separate data and instruction buses to allow data to be loaded from and stored to cache at peak rates of 1 CPI.

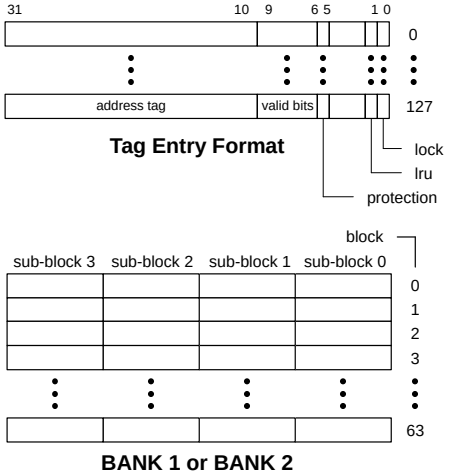


Figure 4. Data Cache Organization

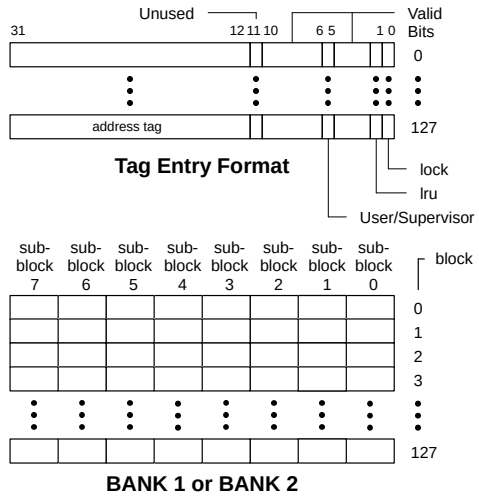


Figure 5. Instruction Cache Organization

FIFOs

The MB86934 provides 6 buffers which are configured as FIFOs. Each of the FIFOs are 64-words deep. The registers for the Enhanced Floating Point instruction set are partially mapped to the FIFOs as follows:

f0-f19, f21, f23, f25, f27, f29, and f31	32-bit register
f20	64-word FIFO A (FA)
f22	64-word FIFO B (FB)
f24	64-word FIFO C (FC)
f26	64-word FIFO D (FD)
f28	64-word FIFO E (FE)
f30	64-word FIFO F (FF)

Each FIFO has a pointer and a depth register associated with it. Any access to the FIFO accesses the location pointed to by the pointer and increments the pointer. When the pointer reaches the value in the depth register, on the next access the pointer rolls over to 0. The FIFOs are also mapped to registers in ASI 0x1 address space. These registers are used by the DMA controller to recognize transfers to and from the FIFOs. These cannot be accessed by LDA/STA instructions.

Any enhanced floating point operation accessing registers f20, f22, f24, f26, f28 and f30 access the head of the corresponding FIFO rather than the corresponding registers. Other Floating Point instructions access the corresponding registers in the floating point register file.

BUS INTERFACE

The SDRAM bus interface is integrated on-chip. This allows the MB86934 to interface to very high performance SDRAMS.

The Bus Interface Unit (BIU) is designed to simplify the interface between the MB86934 and the rest of the system. Separate address and data buses make it easy to build fast systems. At the same time, on-chip circuitry allows these systems to be built with a minimum of external hardware.

Two DMA channels provide high speed memory-to-memory and memory-to-peripheral data transfers. The DMA channels execute independently of the processor and make it possible for the processor to continue to execute from cache while the DMA transfers are taking place. Flexible priority allows the processor to suspend transfers if it needs to use the bus (on a cache miss for example).

The MB86934 DMA controller supports byte, halfword, word and quad-word transfers. Either fly-by or flow-through transfers are possible under single, block and demand transfer modes. Transfers can be chained to support scatter/gather operations. The DMA transfers are initiated either by software or by external hardware handshake.

The DMA controller is capable of transferring data to and from the FIFOs in the fly-by mode.

The bus interface supports fully programmable wait state generation, address decoding with chip select outputs, same page detection to support page-mode DRAM, booting from 8 and 16-bit wide memory, and an auto-reload timer. A burst mode bus supports fast cache line fills.

The BIU can also operate in a mode where the CPU core operates at twice the frequency of the bus interface. This is provided to ease the system design for system where the CPU is running at a high frequency.

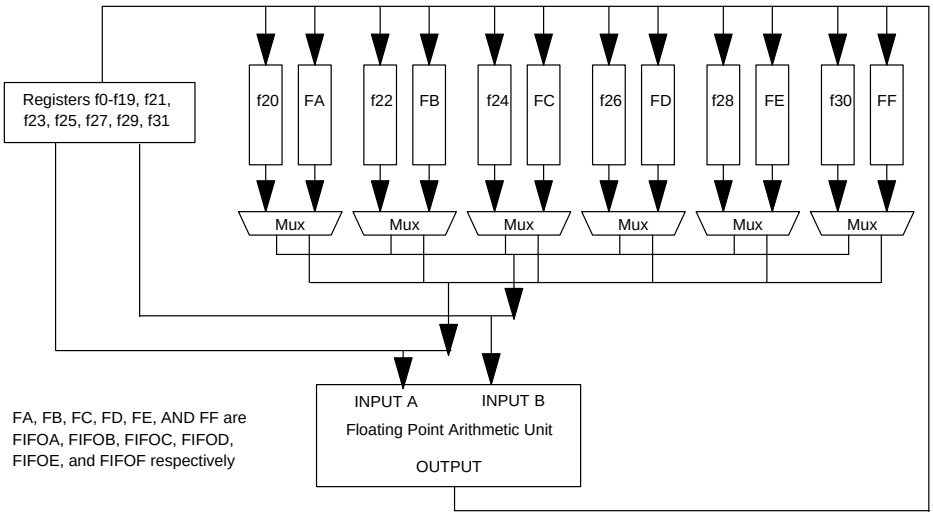
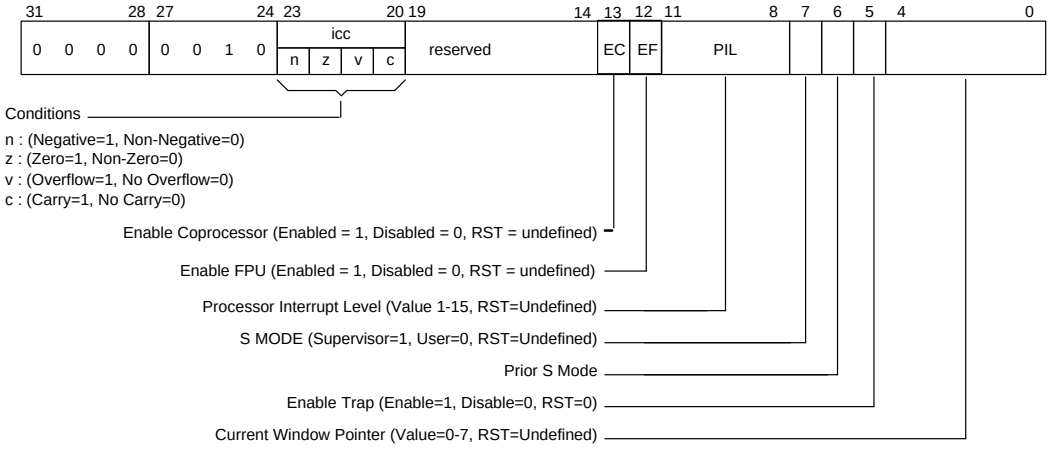


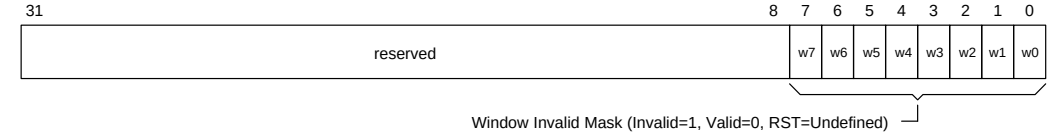
Figure 6: Mapping of FPU registers and FIFOs

Table 2. MB86934 Control and Status Registers (All registers are read/write)

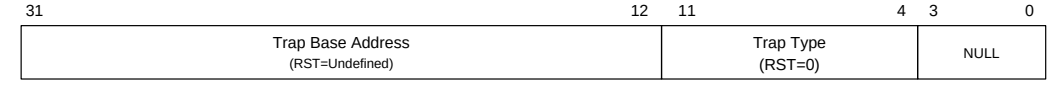
Processor State Register | **PSR**



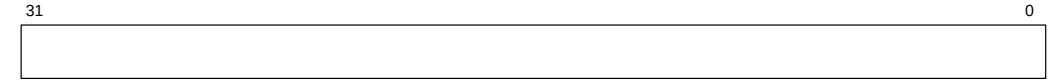
Window Invalid Mask | **WIM**



Trap Base Register | **TBR**



Y Register | **Y**



Ancillary State Register 17 | **ASR 17**

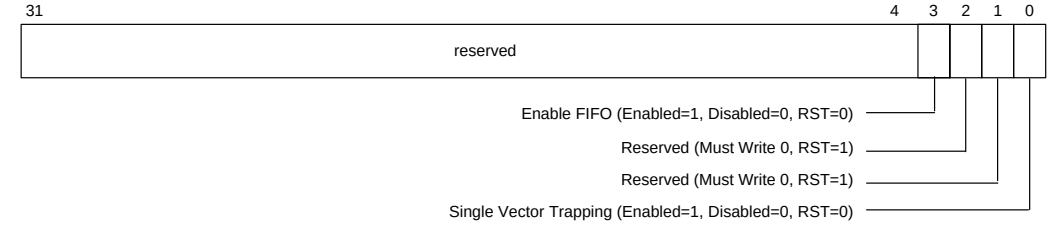
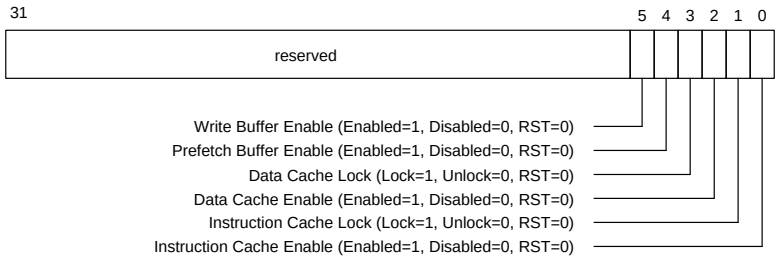


Table 3. MB86934 Memory Mapped Control Registers (All registers are read/write)

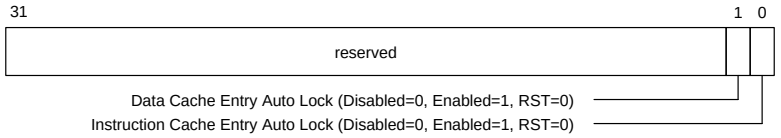
Cache/BIU Control

ASI	ADDRESS
0x 1	0x 0000 0000



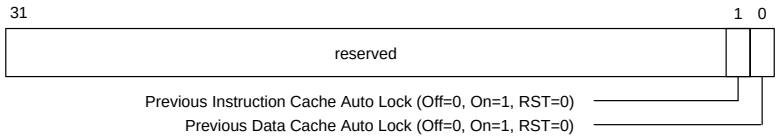
Lock Control

ASI	ADDRESS
0x 1	0x 0000 0004



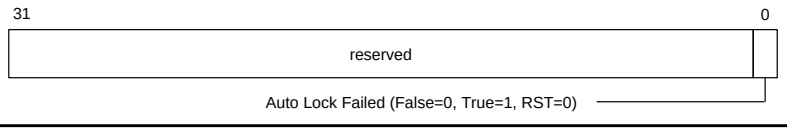
Lock Control Save

ASI	ADDRESS
0x 1	0x 0000 0008



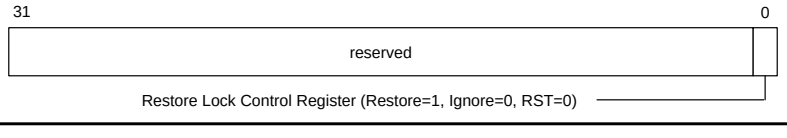
Cache Status

ASI	ADDRESS
0x 1	0x 0000 000C



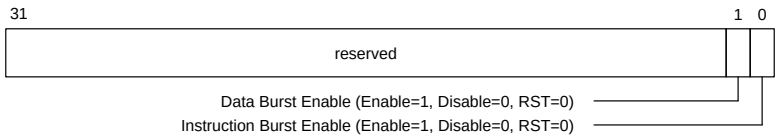
Restore Lock Control

ASI	ADDRESS
0x 1	0x 0000 0010



Bus Control

ASI	ADDRESS
0x 1	0x 0000 0020



System Support Control

ASI	ADDRESS
0x 1	0x 0000 0080

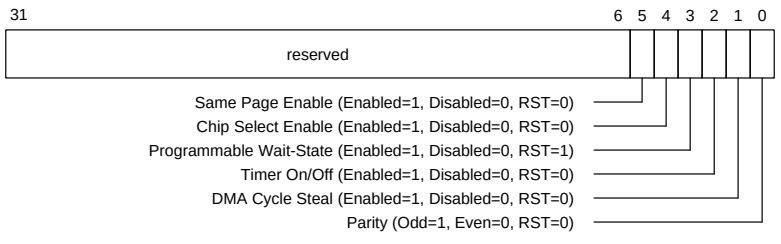
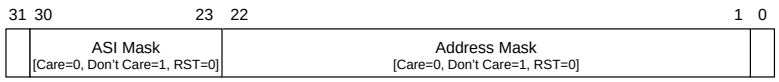


Table 3. MB86934 Memory Mapped Control Registers (Continued)

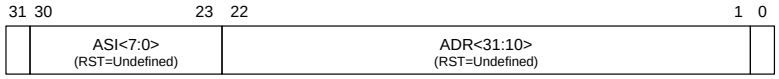
Same Page Mask

ASI	ADDRESS
0x 1	0x 0000 0120



Address Range[1]

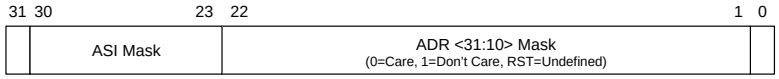
ASI	ADDRESS
0x 1	CS1 0x 0000 0124 CS2 0x 0000 0128 CS3 0x 0000 012C CS4 0x 0000 0130 CS5 0x 0000 0134



NOTE: CS0 is hardwired to ASI=0x9 ADR<31:10> = <0..0>

Address Mask

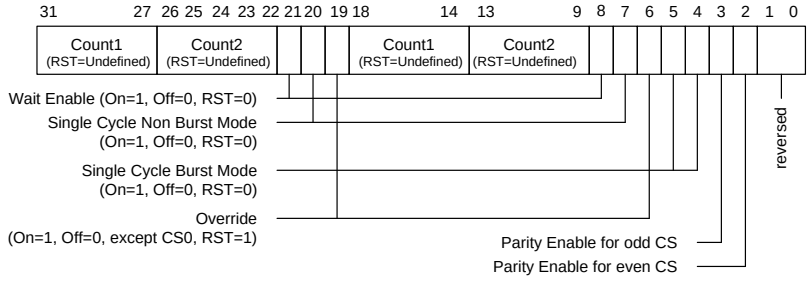
ASI	ADDRESS
0x 1	CS0 0x 0000 0140 CS1 0x 0000 0144 CS2 0x 0000 0148 CS3 0x 0000 014C CS4 0x 0000 0150 CS5 0x 0000 0154



NOTE: CS0 ADR<14:10> = 1, ADR<31:15> = 0, ASI = 0x9 at reset.

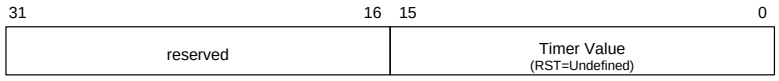
Wait State Specifier

ASI	ADDRESS
0x 1	CS1,CS0 0x 0000 0160 CS3,CS2 0x 0000 0164 CS5,CS4 0x 0000 0168



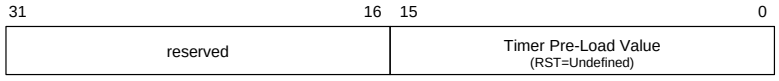
Timer

ASI	ADDRESS
0x 1	0x 0000 0174



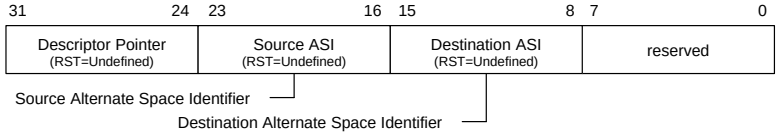
Timer Pre-Load

ASI	ADDRESS
0x 1	0x 0000 0178



Source/Destination ASI

ASI	ADDRESS
0x 1	0x 0000 0180 DMA0 0x 0000 01A0 DMA1

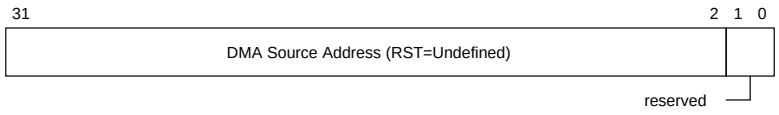


1. This register is Write Only

Table 3. MB86934 Memory Mapped Control Registers (Continued)

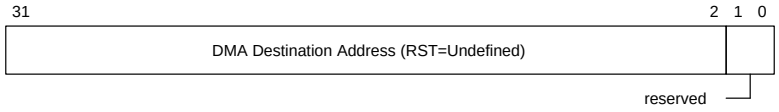
Source Address

ASI	ADDRESS
0x 1	0x 0000 0184 DMA0 0x 0000 01A4 DMA1



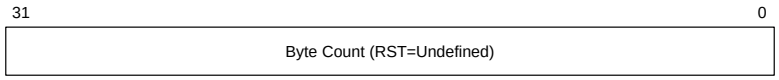
Destination Address

ASI	ADDRESS
0x 1	0x 0000 0188 DMA0 0x 0000 01A8 DMA1



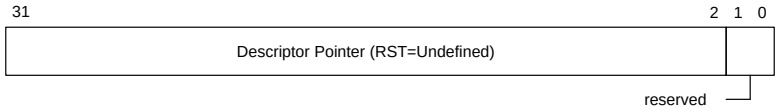
Byte Count

ASI	ADDRESS
0x 1	0x 0000 018C DMA0 0x 0000 01AC DMA1



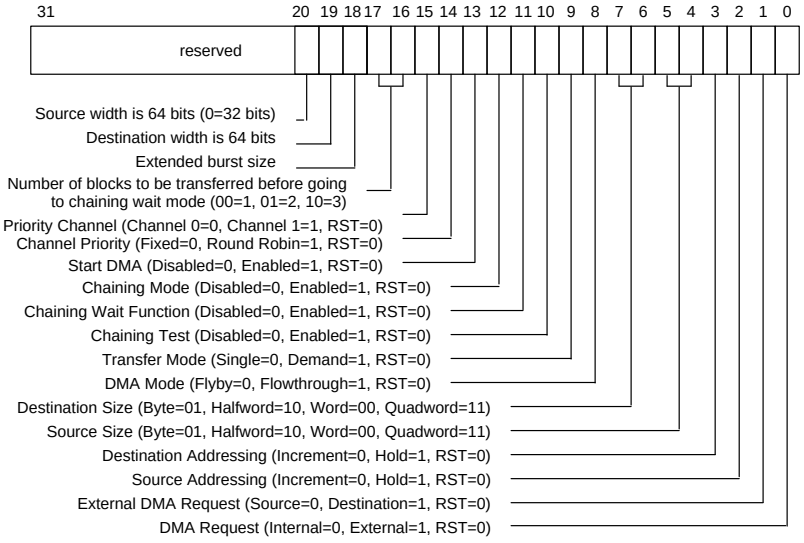
Descriptor Pointer

ASI	ADDRESS
0x 1	0x 0000 0190 DMA0 0x 0000 01B0 DMA1



Channel Control

ASI	ADDRESS
0x 1	0x 0000 0194 DMA0 0x 0000 01B4 DMA1



Channel Status

ASI	ADDRESS
0x 1	0x 0000 0198 DMA0 0x 0000 01B8 DMA1 ASR 0x18 DMA0 ASR 0x19 DMA1

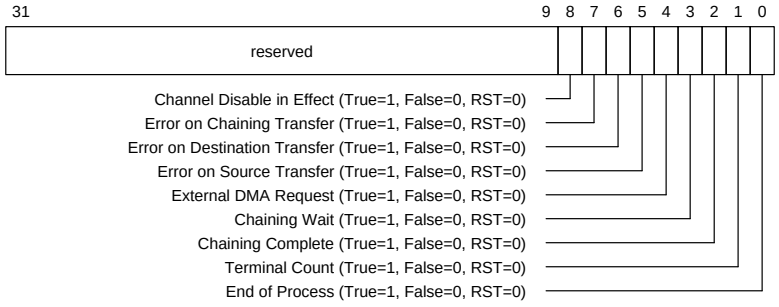
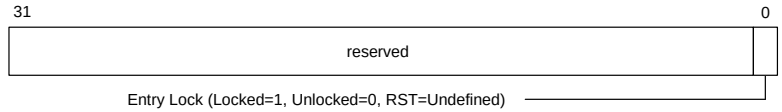


Table 3. MB86934 Memory Mapped Control Registers (Continued)

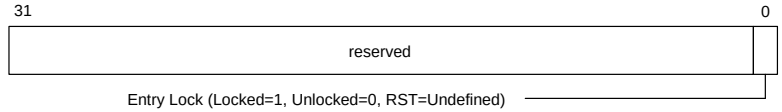
Instruction Tag Lock Bits

ASI	ADDRESS
0x 2	Bank 1 0x 0000 0000 ↓ by 8 words 0x 0000 0FF8 Bank 2 0x 8000 0000 ↓ by 8 words 0x 8000 0FF8



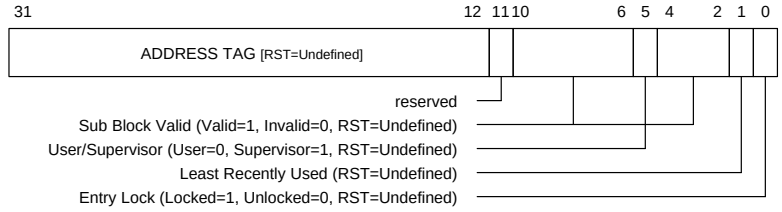
Data Tag Lock Bits

ASI	ADDRESS
0x 3	Bank 1 0x 0000 0000 ↓ by 4 words 0x 0000 03FC Bank 2 0x 8000 0000 ↓ by 4 words 0x 8000 03FC



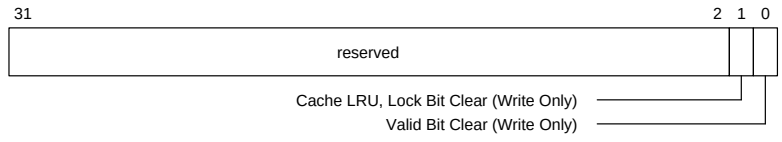
Instruction Cache Tag

ASI	ADDRESS
0x C	Bank 1 0x 0000 0000 ↓ by 8 words 0x 0000 0FF8 Bank 2 0x 8000 0000 ↓ by 8 words 0x 8000 0FF8



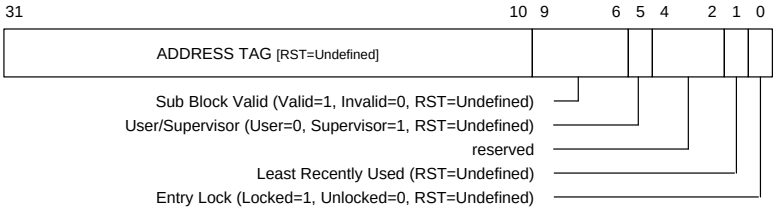
Instruction Cache Invalidate

ASI	ADDRESS
0x C	Bank 1 0x 0000 1000 Bank 2 0x 8000 1000



Data Cache Tag

ASI	ADDRESS
0x E	Bank 1 0x 0000 0000 ↓ by 4 words 0x 0000 03FC Bank 2 0x 8000 0000 ↓ by 4 words 0x 8000 03FC



Data Cache Invalidate

ASI	ADDRESS
0x E	Bank 1 0x 0000 1000 Bank 2 0x 8000 1000

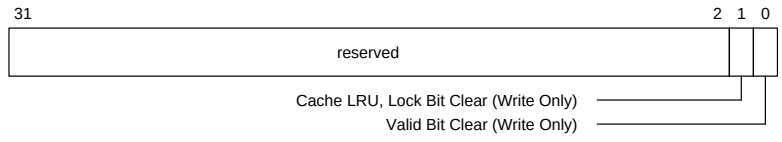
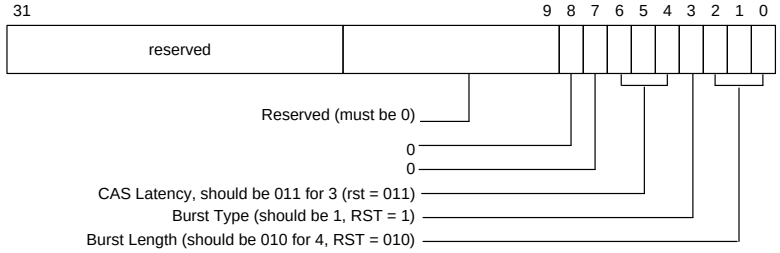


Table 3. MB86934 Memory Mapped Control Registers (Continued)

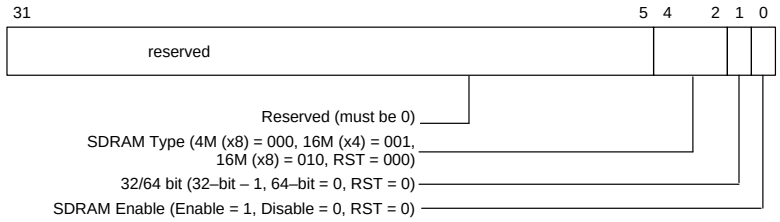
Instruction Cache Data		
ASI	ADDRESS	
0x D	Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400 Bank 2 0x 0000 0000 ↓ by 1 word 0x 8000 0400	31 … 0 ADDRESS TAG [RST=Undefined]
Data Cache Data		
ASI	ADDRESS	
0x F	Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 1 word 0x 8000 0400	31 … 0 ADDRESS TAG [RST=Undefined]
FIFO Pointer		
ASI	ADDRESS	
0x I	0x 500, 0x 504 0x 508, 0x 50C 0x 510, 0x 514 for FIFO A to FIFO F respectively	31 … 8 7 … 2 1 0 reserved word address reserved reserved
FIFO Depth Register		
ASI	ADDRESS	
0x I	0x 518, 0x 51C 0x 520, 0x 524 0x 528, 0x 52C for FIFO A to FIFO F respectively	31 … 8 7 … 2 1 0 reserved word length reserved reserved
FIFO		
ASI	ADDRESS	
0x I	0x 530, 0x 534 0x 538, 0x 530 0x 540, 0x 544 for FIFO A to FIFO F respectively	31 … 0 reserved

Table 3. MB86934 Memory Mapped Control Registers (Continued)

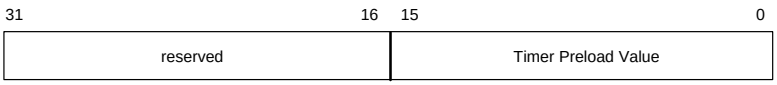
SDRAM Mode Register	
ASI	ADDRESS
0x 1	0x 600



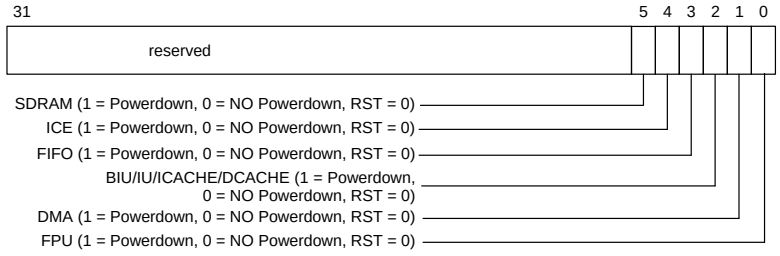
SDRAM Enable Register	
ASI	ADDRESS
0x 1	0x 604



SDRAM Refresh Timer	
ASI	ADDRESS
0x 1	0x 608



Power Down Register	
ASI	ADDRESS
0x 1	0x 60



BUS OPERATION

The Bus Interface Unit (BIU) has the logic which allows the MB86934 to interface with the system. The system interface is made up of the address and data buses, the interrupt request bus and various control signals. The BIU is either handling requests for external memory operations, arbitrating for bus access, or idle.

Operation of the BIU

In the case of a write to external memory, the BIU makes use of a write buffer which can hold a one word write transaction. When the BIU receives a request for a write transaction it stores the write data and address in the write buffer allowing the IU to continue operating out of on-chip cache and/or its register file. The BIU then proceeds to complete the write to external memory. In most cases the write buffer will hide external memory latency from the IU. The exceptions are in cases where the write buffer is still filled from a previous transaction or if the subsequent IU cycle results in an instruction cache miss. In these cases, IU execution is held until the write buffer is emptied.

The BIU includes a one stage prefetch buffer for instruction fetches. This buffer is used to fetch the next sequential instruction after an instruction cache miss. The instruction is prefetched only if the BIU does not have a request for a bus transaction from the IU nor is any external device requesting use of the bus. The prefetch buffer operation is suspended if the buffer is full. This occurs if the prefetched instruction is a hit in the instruction cache. The buffer restarts after another instruction cache miss. If an exception occurs during an instruction prefetch, the exception is not sent to the IU unless the instruction is actually requested by the IU. The prefetch buffer operates only when the instruction cache is on and burst mode is disabled.

In any cycle the BIU can receive a request for accesses to either or both instruction and/or data memory. If it receives a request for both in the same cycle, it completes the data memory transaction first.

Exception Handling

The external memory system can indicate an exception during a memory operation. Parity errors cause an exception as well. The BIU signals the appropriate data or instruction exception to the IU which will trap accordingly.

As mentioned above, the IU can continue operation after putting the data and address for a store in the write buffer. If an exception is detected while completing this buffered write, then the BIU indicates a data access exception to the IU.

Any system which needs to recover from this error should store the address and data of such write transactions in hardware. If the system can generate both read and write exceptions, then the system must also provide a status bit which indicates whether the exception was generated on a read or on a write transaction. With access to this information the data access exception service routine can determine the cause of the exception and recover accordingly.

Bus Cycles

Timings 1 through 18 illustrate representative combinations of bus cycles.

Load

Whenever an instruction fetch or a load from data memory has a miss in the cache, the BIU performs a read from external memory.

A read transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de-asserted after one cycle. At the same time the ADR<31:2> and ASI<3:0> bits are driven with the location to be read. The BIU drives the RD/–WR signal high to indicate a read transaction.

The external memory system responds with the read data on pins D<31:0>. It also asserts the –READY signal when the data is ready. For slow memory, the –READY signal can be delayed until data is valid.

A load double operation is treated as back-to-back reads.

Load with Exception

If the external memory system sees a memory exception it can terminate the current memory transaction by asserting the –MEXC and –READY signals. The data on the data bus is ignored by the MB86934.

Store

A write transaction begins with the BIU asserting –AS, to indicate a new bus transaction. At the same time the ADR<31:2> and ASI<3:0> pins are driven with the location to be written while the D<31:0> pins has corresponding write data. The –BE0-3 pins indicate byte, half-word or word transaction width. The BIU drives the RD/–WR signal low to indicate a write transaction. The –AS signal is de-asserted after one phase.

The external memory system responds by asserting the –READY signal when it has stored the data.

A store double operation is treated as back-to-back writes.

Store with Exception

If an access exception occurs on a write, the external memory system can terminate the current memory transaction by asserting the –MEXC and –READY signals. The external memory system is expected to ignore the data on the data bus in this situation.

Atomic Load Store

An atomic load store executes as a load followed by a store with no operation allowed in between. The –LOCK signal is asserted to indicate that the bus is being used for more than one external memory operation.

There is one cycle between the termination of the read and the beginning of the write to provide time for the switching of the data bus drivers.

External Bus Request and Grant

Any external device can request ownership of the bus by asserting the –BREQ signal. The BIU asserts the –BGRNT signal to indicate that it is relinquishing control of the bus and also three-states all of its bus drivers. In the following cycle, the external device can begin its transaction. On completion of its transaction the external device de-asserts the –BREQ signal. The BIU responds by de-asserting the –BGRNT signal in the following cycle.

A separate signal, –PBREQ, is asserted by the processor to indicate to a bus arbiter that it needs the bus back. This allows the bus to be allocated based on demand.

The MB86934 is the default owner of the bus.

8-Bit and 16-Bit Bus Modes

The MB86934 supports chip select zero (CS0 to be mapped into memory that can be either 8, 16, or 32-bits wide). Memory width for CS0 is selected at system reset.

Transactions of 8 and 16-bit widths are similar to 32-bit transactions except that –AS is asserted only once at the beginning of the bus cycle and –READY is asserted after each byte or halfword is available. –BE[0:3] indicates the byte or halfword being read or written (see Timing diagrams 8 and 9).

Burst Mode Transactions

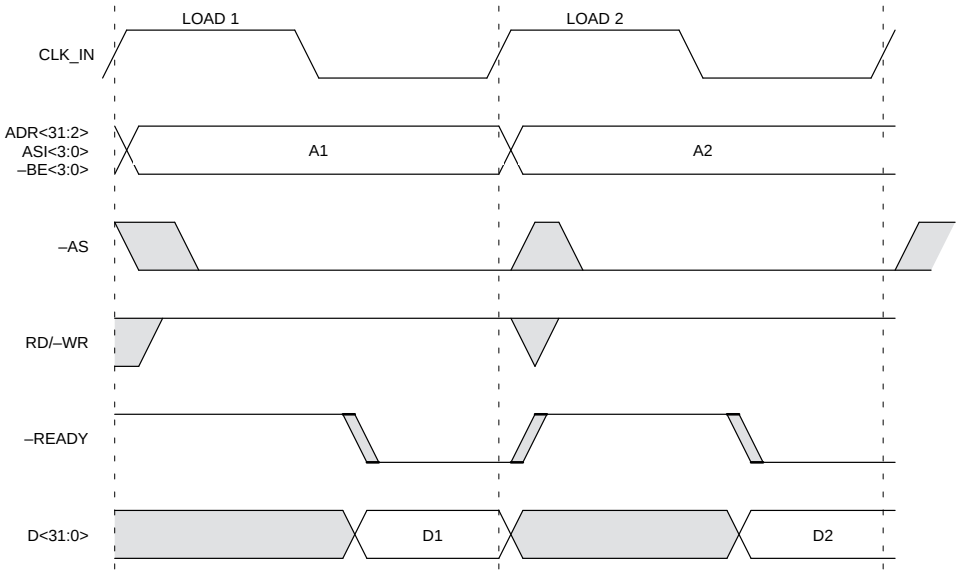
For systems that can support burst mode transactions, the MB86934 can be programmed to support 4 word bursts. When burst mode is enabled, –BMREQ is asserted at the beginning of each bus cycle for which a burst access can be done (see timing diagram 9). If the memory system can support a burst for the current bus address, it asserts –BMACK to begin the burst transaction. –BMACK is asserted on the first word of the burst transaction only. –READY is asserted with each word of the burst. Systems that do not support burst mode for the current address should not assert –BMACK (see timing diagram 10 and 11). If –BMREQ is not asserted for a transaction the memory should return only one word.

Direct Memory Access

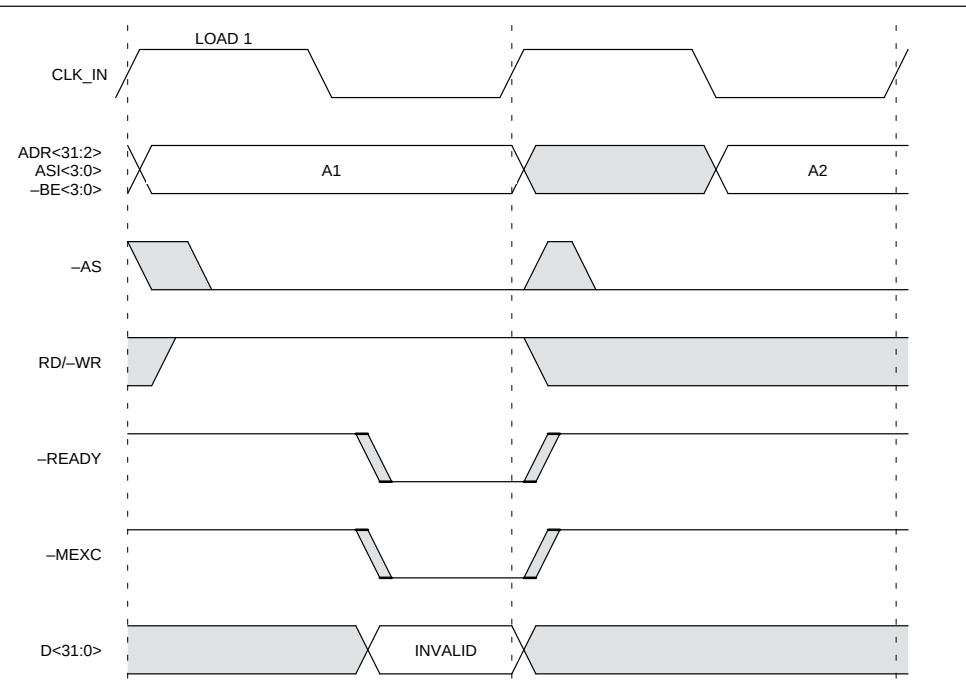
For systems that can support burst mode transactions, the MB86934 can support a number of different DMA modes. (See timing diagrams 12 through 16 for details.)

SDRAM

For timing diagrams for SDRAM read and writes please see figures 17 and 18.

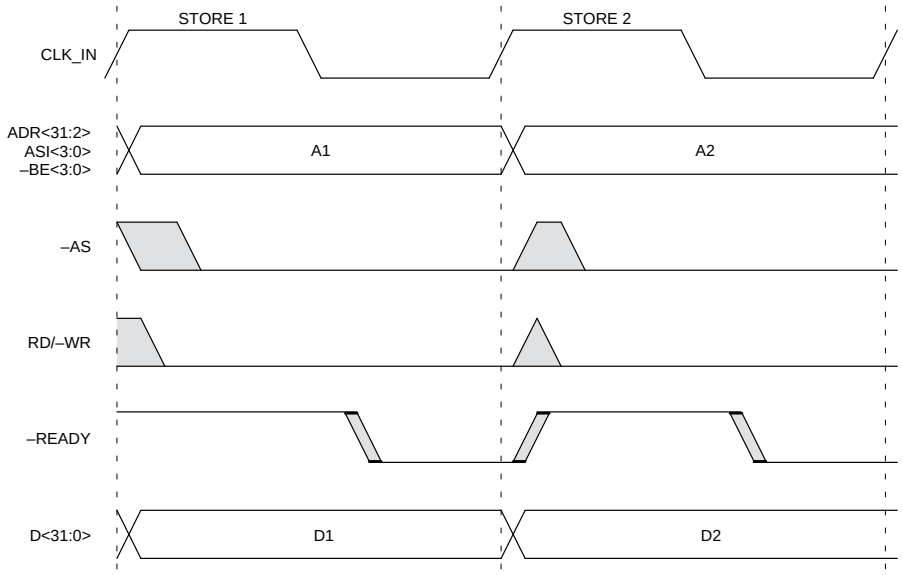


Timing 1. Back-to-Back Loads (LDDF)*

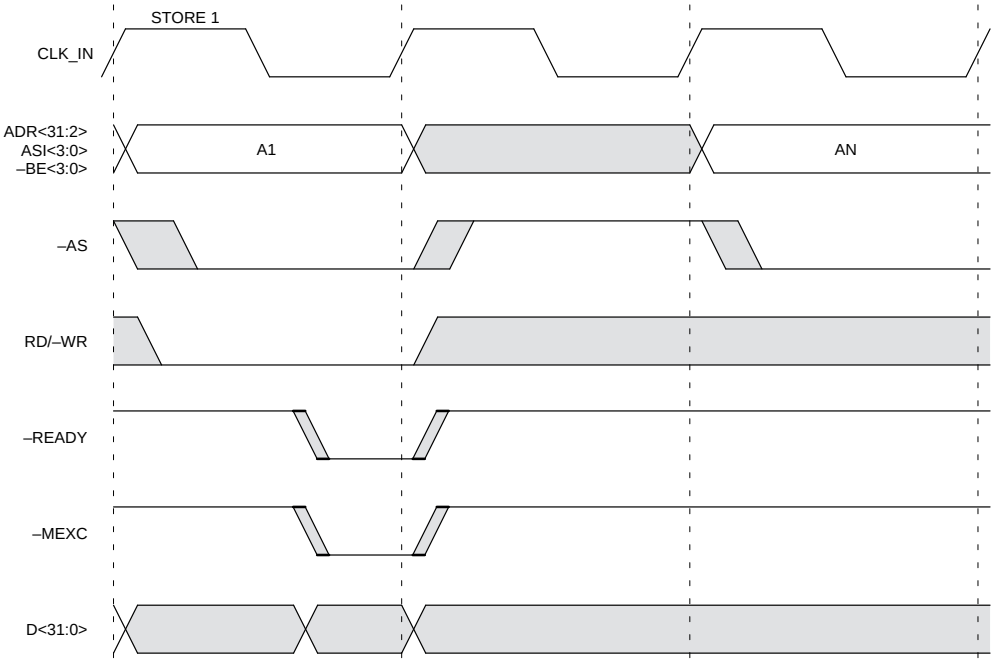


Timing 2. Load with Exception

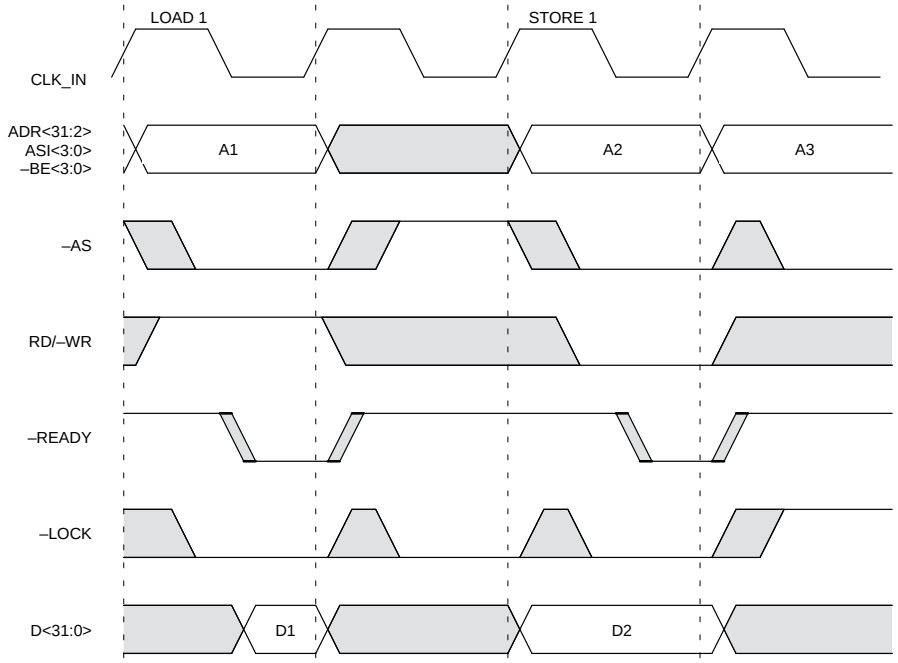
* Back to back loads have at least one intervening idle clock. However, LDDF will do true back to back cycles.



Timing 3. Typical Back-to-Back Stores (Same as Store Double)

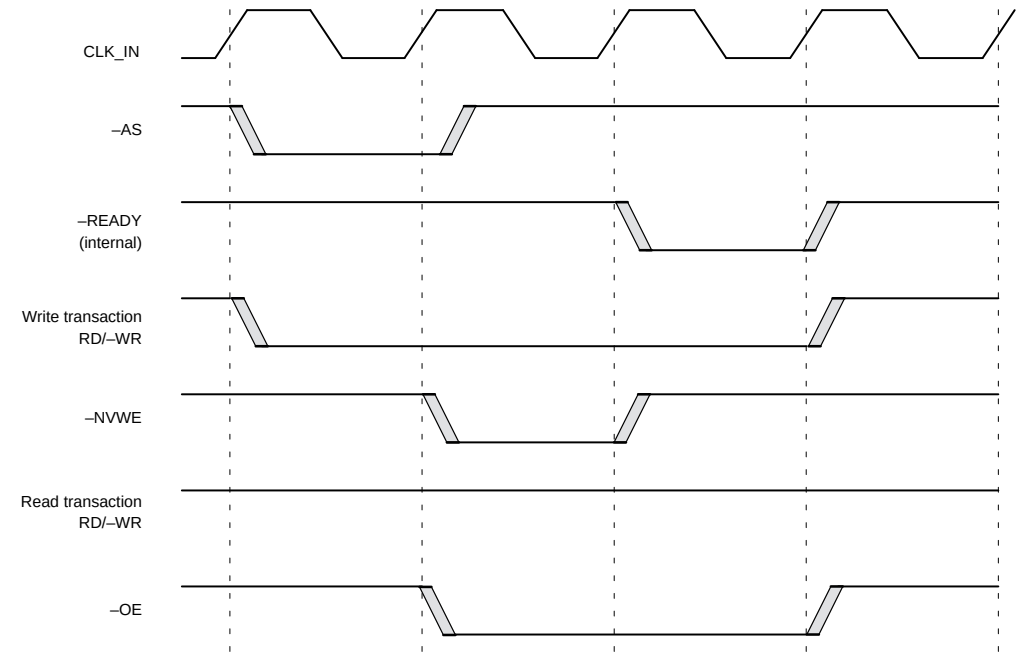


Timing 4. Store with Exception

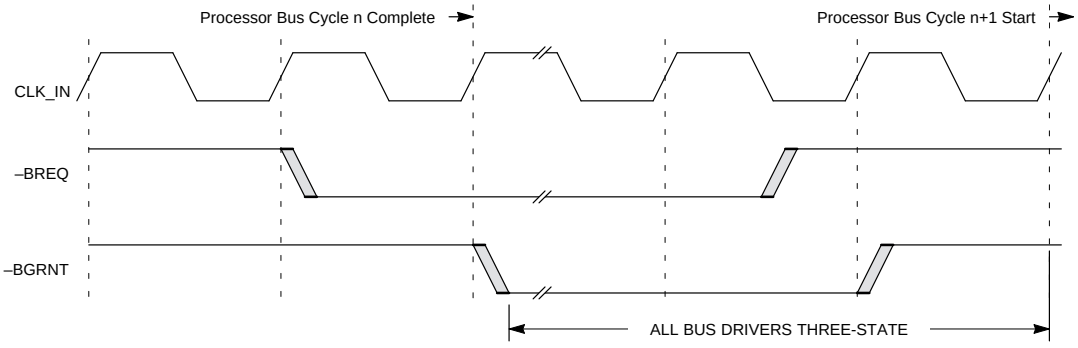


Note: A load followed by a store requires an intervening clock cycle on the bus while a store followed by a load can occur in consecutive clock cycles.

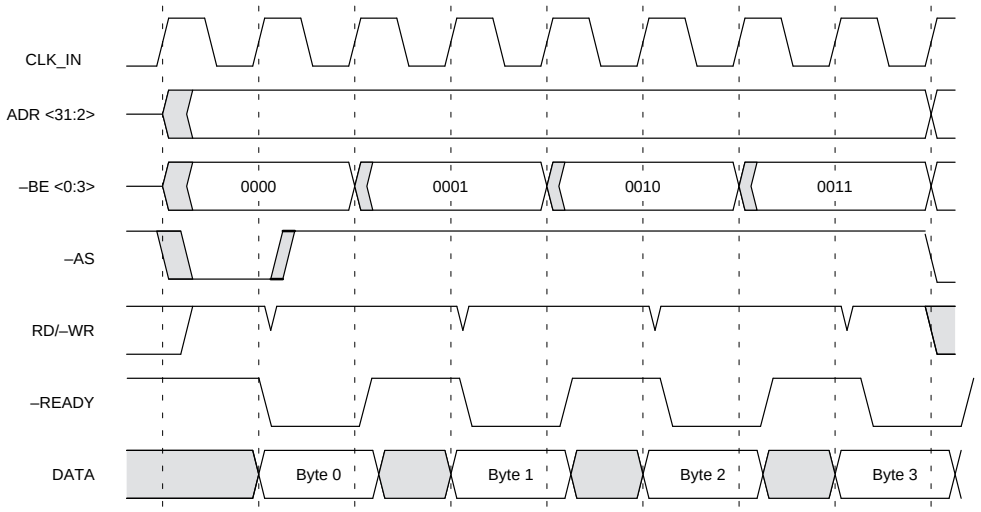
Timing 5. Atomic Operation



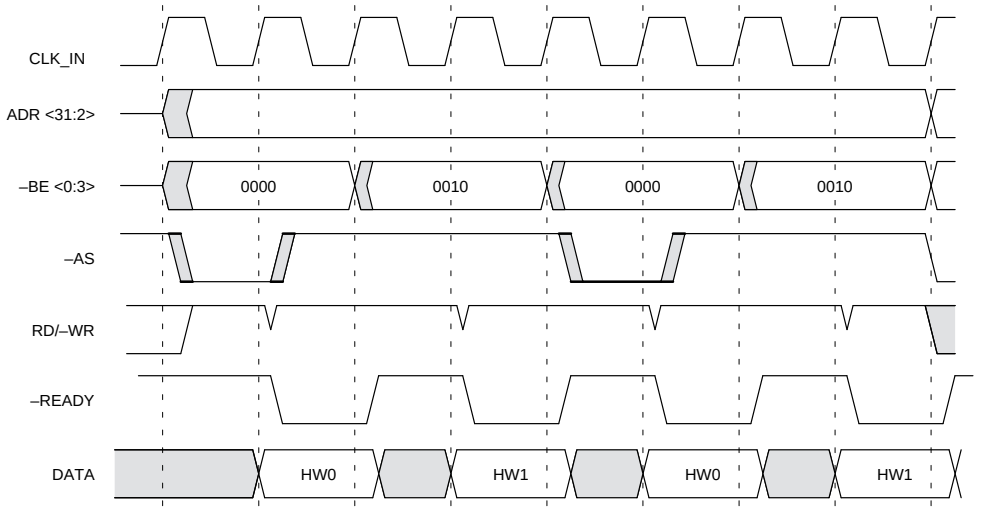
Timing 6. Timing for –NVWE and –OE



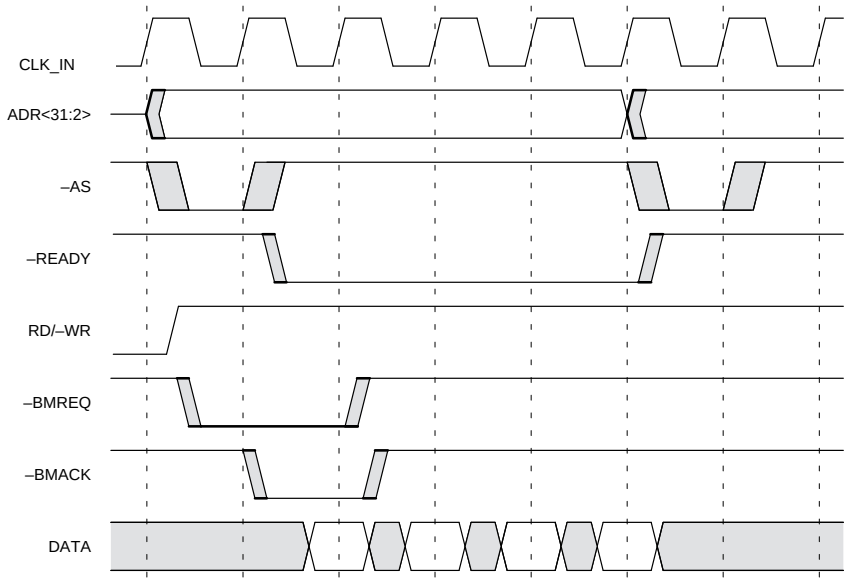
Timing 7. Bus Request and Grant Cycle



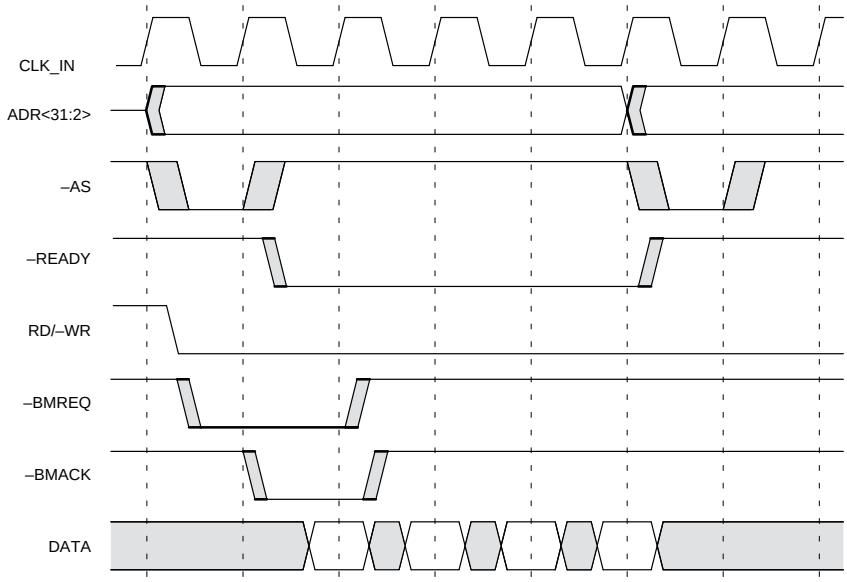
Timing 8. 8-Bit Bus Mode (1 Wait State)



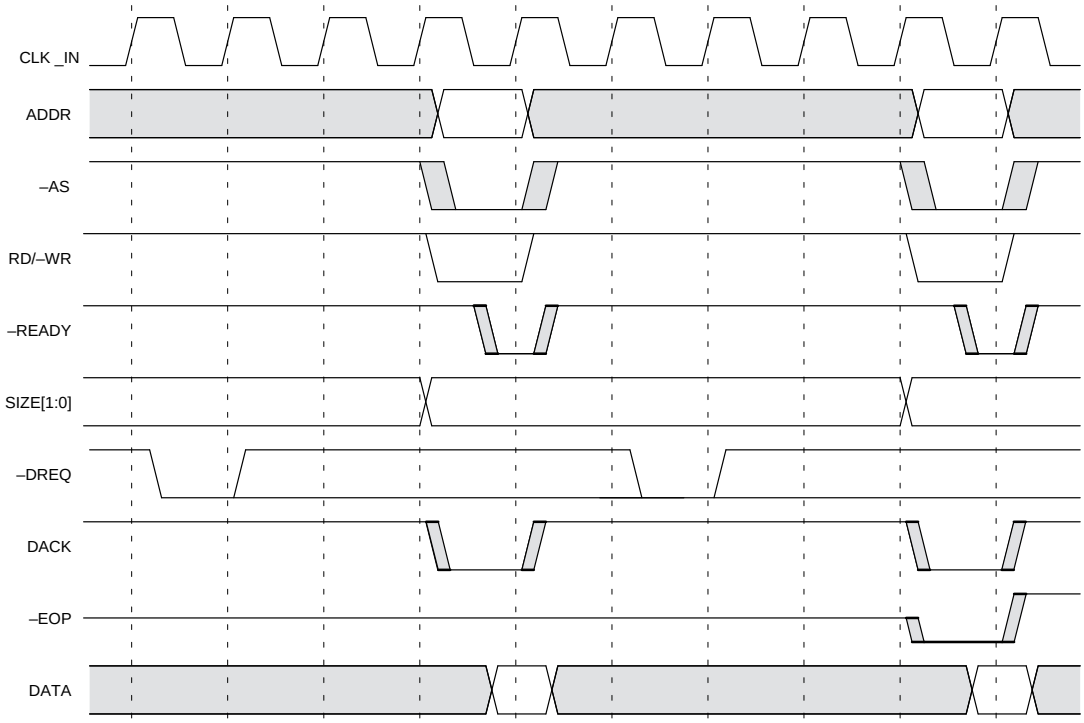
Timing 9. 16-Bit Bus Mode (1 Wait State)



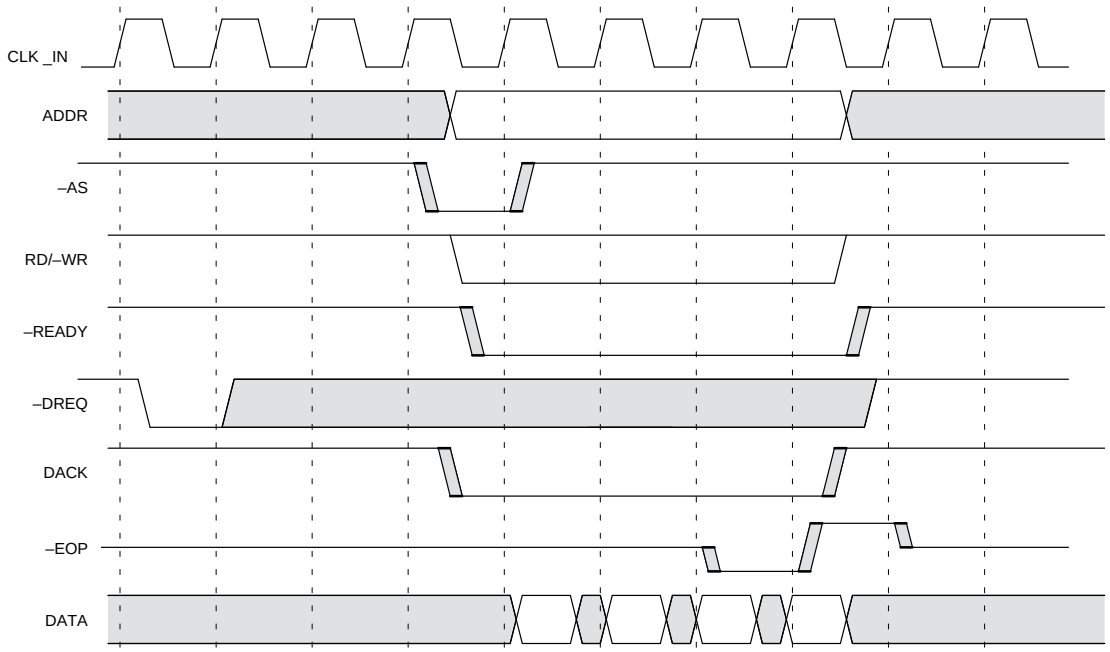
Timing 10. Burst Mode Read



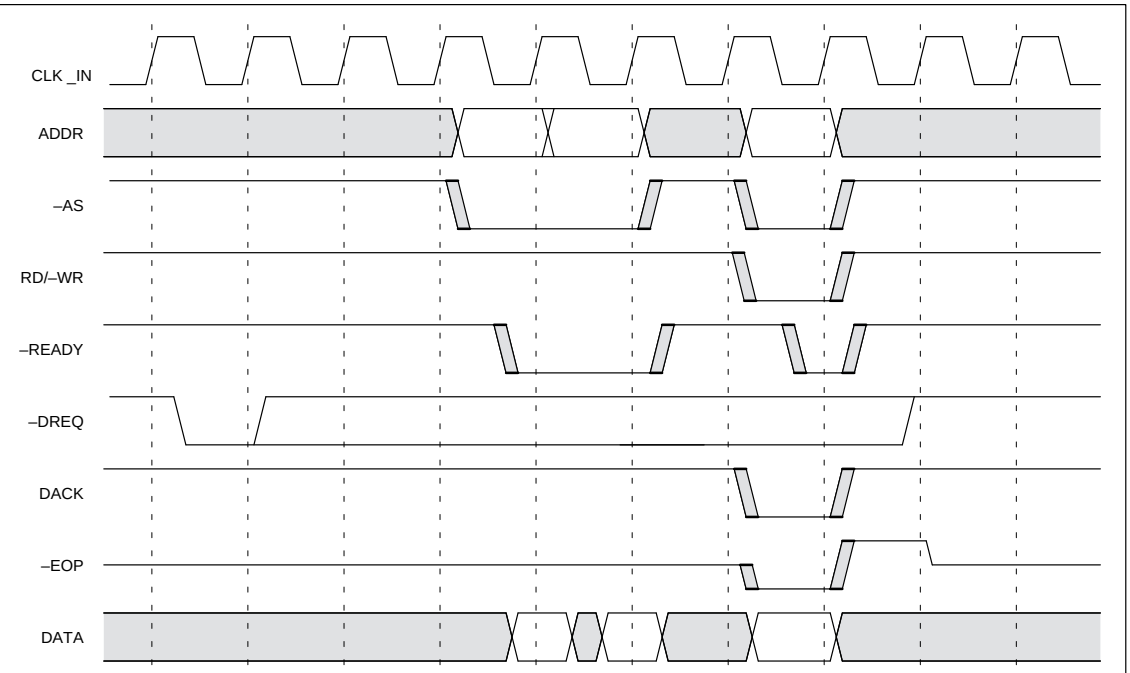
Timing 11. Burst Mode Write (DMA Only)



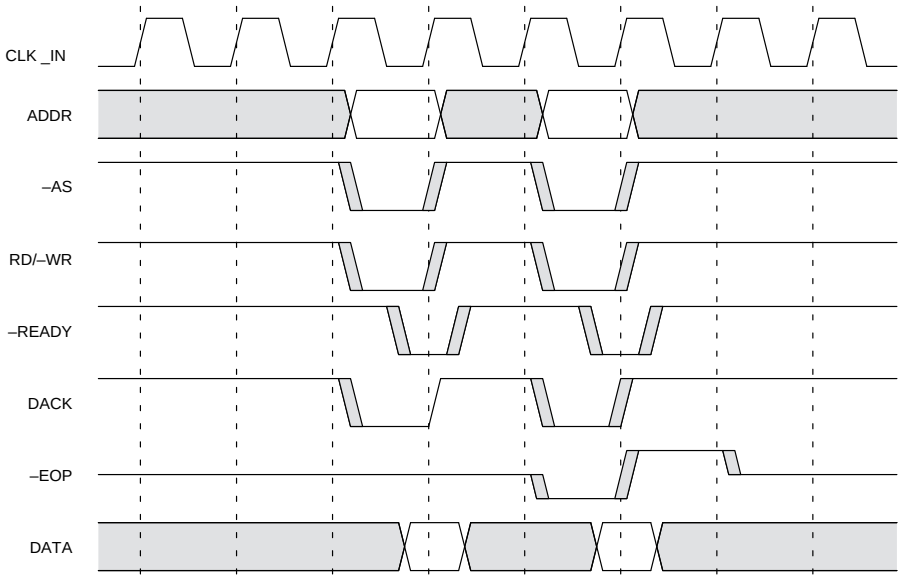
Timing 12. Single Transfer, Edge Sensitive, Flyby



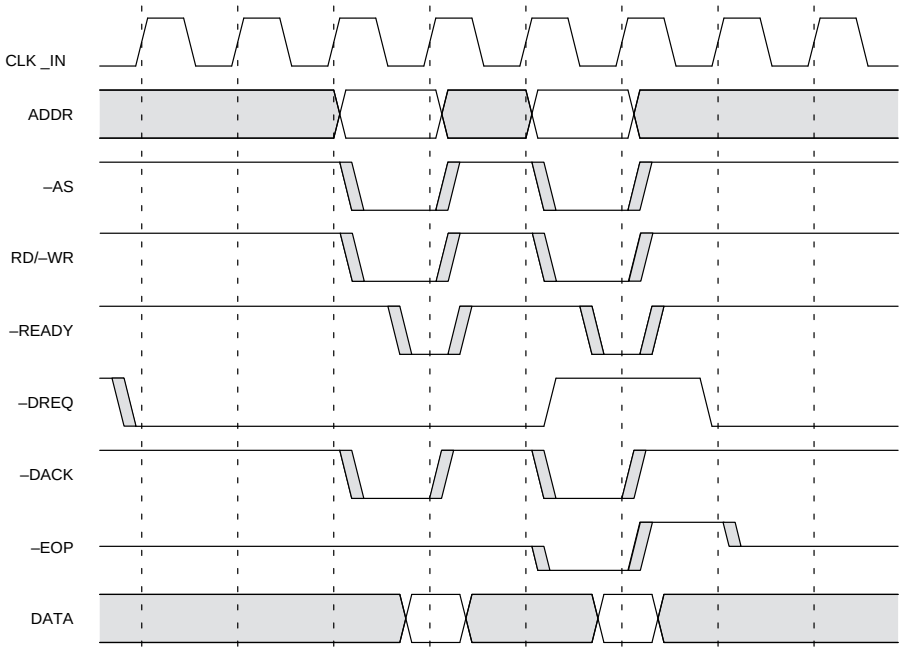
Timing 13. Single Transfer, Edge Sensitive, Flyby, Quadword



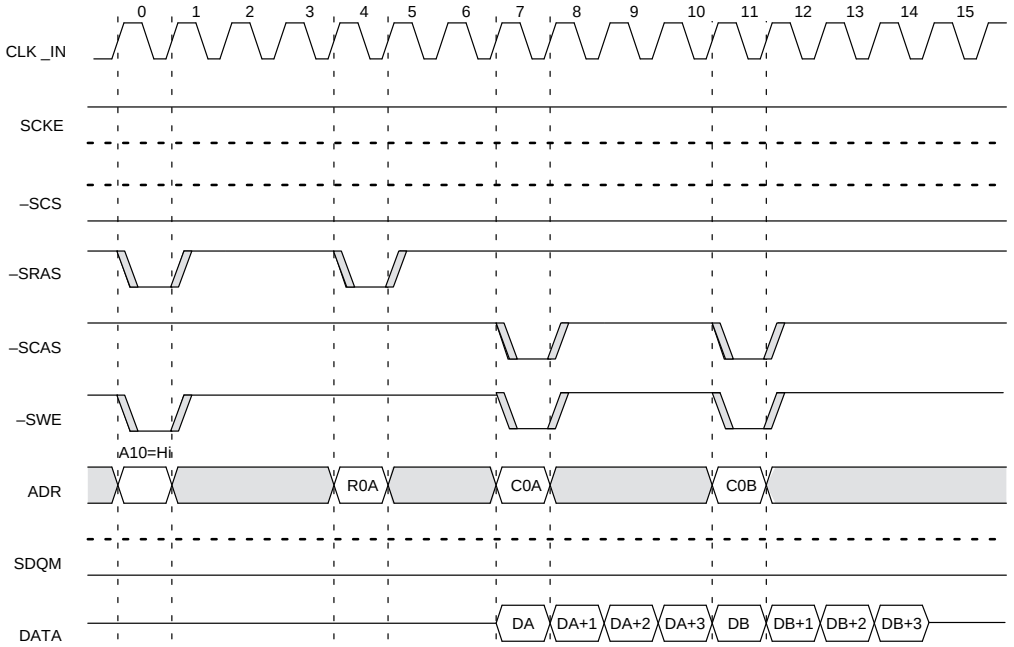
Timing 14. Single Transfer, Edge Sensitive, Flowthru, Dest Request (half–word source, word destination)



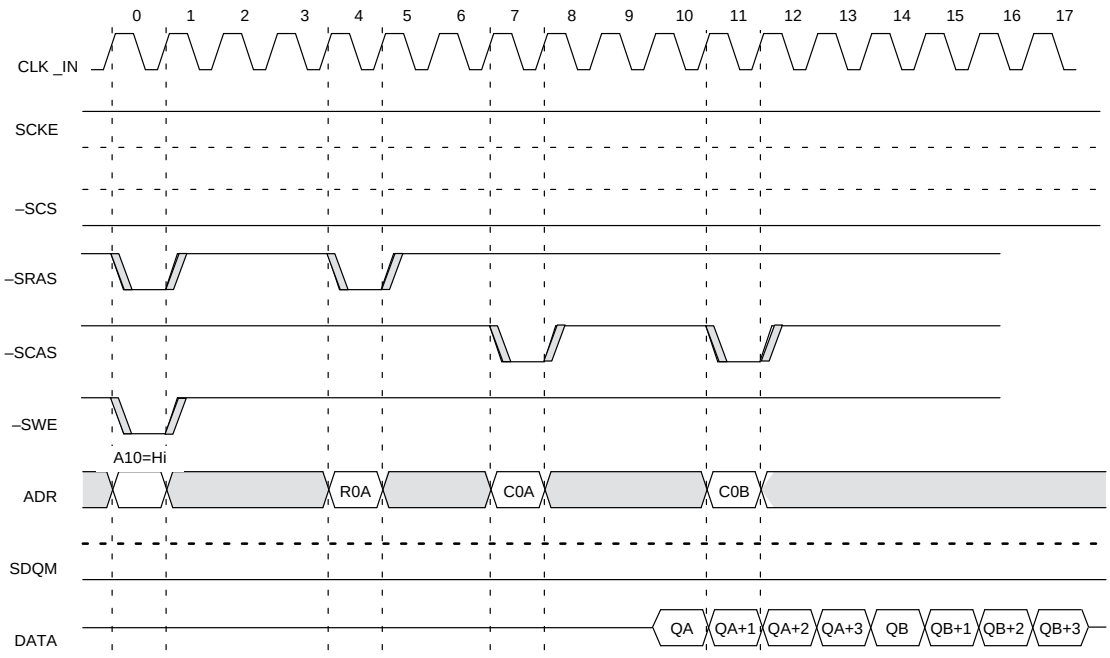
Timing 15. Block Transfer, Flyby



Timing 16. Demand Transfer, Flyby



Timing 17. Random Column Burst Write Cycle



Timing 18. Random Column Burst Read Cycle

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Conditions	Min.	Max.	Units
V_{DD}	Supply voltage		–0.3	4	V
A_V_{DD}	Analog (PLL) Voltage		–0.3	4	V
IO_V_{DD}	I/O (Pin) Voltage		–0.3	6	V
V_I	Input voltage		–0.3	IO_V_{DD} + 0.3	V
T_J	Operating junction temperature			125	°C

1. Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Connections:

1. Power and ground connections must be made to multiple V_{DD} and V_{SS} pins. Every MB86934 based circuit board should include power (V_{DD}) and ground (V_{SS}) planes for power distribution. Every V_{DD} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified a “N.C.” must not be connected in the system.
2. Liberal decoupling capacitance should place near the MB86934. The processor can cause transient power surges when its numerous output buffers transition particularly when connected to large capacitance loads.
3. Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for QFP packages will offer the lowest possible inductance.
4. For reliable operation, alternate bus masters must drive any pins that are three-stated by the MB86934 when it granted the bus, in particular –LOCK, ADR<31:1>, ASI<3:0>, –BE0-3, D<31:0>, –AS, and RS/–WR must be driven by alternate bus masters. These pins are normally driven by the processor during active and idle bus states and don’t require external pullups. N.C. pins must always remain unconnected.

PACKAGE THERMAL CHARACTERISTICS (TYPICAL)

Symbol	Parameter	Package	Value			Units
$\varnothing_{JC}$	Thermal resistance junction to case	256 Ceramic QFP	2.1			°C/W
			0 m/s	1 m/s	3 m/s	
$\varnothing_{JA}$	Thermal resistance junction to ambient	256 Ceramic QFP	15	12	10	°C/W

DC SPECIFICATIONS[3] V_{DD} = 3.3V ± 5%, A_V_{DD} = 3.3V ± 5%, IO_V_{DD} = 3.3V ± 5% or = 5V ± 5%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage		0	—	0.8	V
V_{IH}	Input high voltage		2.0	—	IO_V_{DD}	V
V_{OL}	Output low voltage	I_{OL} = 0.8mA	0	—	0.45	V
V_{OH}	Output high voltage	I_{OH} = –0.8mA	2.4	—	IO_V_{DD}	V
I_{LI}	Input leakage current	V_{IN} = 0 or IO_V_{DD}	–10	—	10	µA
I_{LZ}	3–state output leakage current	V_{OUT} = 0 or IO_V_{DD}	–10	—	10	µA
C_{PIN}	Pin capacitance (All pins except XTAL2)		—	—	13	pF
	Pin capacitance (Pin XTAL2)		—	—	16	pF

POWER CONSUMPTION V_{DD} = 3.3V ± 5%, A_V_{DD} = 3.3V ± 5%, IO_ V_{DD} = 3.3V ± 5% or = 5V ± 5%

Symbol	Parameter	Conditions		Typ.	Max.	Units
I_{DD}	Operating power supply current	50 MHz (internal clock)		440	660	mA
A_I_{DD}	Analog (PLL) current	50 MHz (internal clock)		1	1.5	mA
IO_I_{DD}	I/O (Pin) current (In Clock Doubler Mode)	25 MHz (external clock), 30 pF load, IO_ V_{DD} = 3.3V	*1	60	90	mA
			*2	30	45	
			*3	15	22.5	
		25 MHz (external clock), 30 pF load, IO_ V_{DD} = 5V	*1	100	150	mA
			*2	50	75	
			*3	25	37.5	

(*1) Store intensive program, Zero wait state
(*2) Store intensive program, Two wait states
(*3) Cache intensive program, Cache ON

AC CHARACTERISTICS[1,2,4,5], T_A 0–70°C, IO_ V_{DD} = 3.3V ± 5% or = 5V ± 5%, V_{DD} = 3.3V ± 5%, A_V_{DD} = 3.3V ± 5%

Symbol	Parameter Description		Min.	Max.	Units
t1	CLK_IN Period (in clock doubler mode)		40	100	ns
t2	CLK_IN High Time		10		ns
t3	CLK_IN Low Time		10		ns
t4	CLK_IN Rise Time			2	ns
t5	CLK_IN Fall Time			2	ns
t10	D<31:0>	Output Valid Delay		18	ns
		Output Hold	2		
t11	PARITY<3:0>	Output Valid Delay		21	ns
		Output Hold	2		
t12	ADR<31:2>	Output Valid Delay		21	ns
		Output Hold	2		
t13	–BE0-3	Output Valid Delay		20	ns
		Output Hold	2		
t14	ASI <3:0>	Output Valid Delay		15	ns
		Output Hold	2		
t15	–CS0 — –CS4	Output Valid Delay		16	ns
		Output Hold	2		
t16	–SAME_PAGE	Output Valid Delay		17	ns
		Output Hold	2		
t17	RD/–WR	Output Valid Delay		14	ns
		Output Hold	2		
t18	–LOCK	Output Valid Delay		15	ns
		Output Hold	2		
t19	–AS	Output Valid Delay		13	ns
		Output Hold	2		
t20	–TIMER_OVF	Output Valid Delay		15	ns
		Output Hold	2		

AC CHARACTERISTICS[1,2,4,5] T_A 0–70°C, IO_ V_{DD} = 3.3V ± 5% or = 5V ± 5%, V_{DD} = 3.3V ± 5%, A_V_{DD} = 3.3V ± 5% (Continued)

Symbol	Parameter Description		Min.	Max.	Units
t21	–BGRNT	Output Valid Delay		14	ns
		Output Hold	2		
t22	–DACK0, –DACK1	Output Valid Delay		15	ns
		Output Hold time	2		
t23	–EOP0, –EOP1	Output Valid Delay		15	ns
		Output Hold	2		
t24	–BMREQ	Output Valid Delay		15	ns
		Output Hold	2		
t25	–PBREQ	Output Valid Delay		13	ns
		Output Hold	2		
t26	–SWE	Output Valid Delay		13	ns
		Output Hold	2		
t27	–SRAS	Output Valid Delay		13	ns
		Output Hold	2		
t28	–SCAS	Output Valid Delay		13	ns
		Output hold	2		
t29	–SCS0, –SCS1, –SCS2, –SCS3	Output Valid Delay		13	ns
		Output Hold	2		
t30	SCKE	Output Valid Delay		13	ns
		Output Hold	2		
t31	SDQM0, SDQM1	Output Valid Delay		13	ns
		Output Hold	2		
t32	–NVWE	Output Valid Delay		15	ns
		Output Hold	2		
t33	–OE	Output Valid Delay		13	ns
		Output Hold	2		
t34	–READYOUT	Output Valid Delay		14	ns
		Output Hold	2		

AC CHARACTERISTICS[1,2,4,5] T_A 0–70°C, IO_ V_{DD} = 3.3V ± 5% or = 5V ± 5%, V_{DD} = 3.3V ± 5%, A_V_{DD} = 3.3V ± 5% **(Continued)**

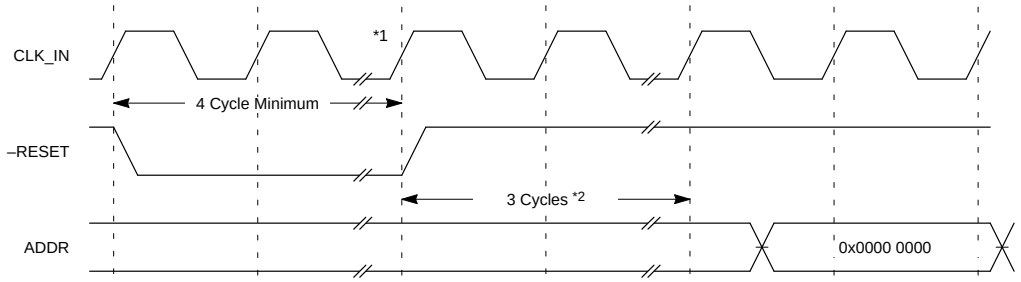
Symbol	Parameter Description		Min.	Max.	Units
t40	–MEXC	Input Setup Time	12		ns
		Input Hold Time	2		
t41	–READY	Input Setup Time	14		ns
		Input Hold Time	2		
t42	D<31:0>	Input Setup Time	16		ns
		Input Hold Time	2		
t43	PARITY <3:0>	Input Setup Time	16		ns
		Input Hold Time	2		
t44	–BREQ	Input Setup Time	8		ns
		Input Hold Time	2		
t45	–DREQ0, –DREQ1	Input Setup Time	6		ns
		Input Hold Time	2		
t46	–EOP0, –EOP1	Input Setup Time	4		ns
		Input Hold Time	2		
t47	–BMACK	Input Setup Time	9		ns
		Input Hold Time	2		
t48	–AS	Input Setup Time	13		ns
		Input Hold Time	2		
t49	ADR<31:2>	Input Setup Time	9		ns
		Input Hold Time	2		
t50	ASI <3:0>	Input Setup Time	4		ns
		Input Hold Time	2		
t51	RD/–WR	Input Setup Time	4		ns
		Input Hold Time	2		

Timing for Data and Address with SDRAM Interface

Symbol	Parameter Description		Min.	Max.	Units
t60	D<63:0>	Output valid delay		16	ns
		Output hold	2		
t61	ADR<15:2>	Output valid delay		13	ns
		Output hold	2		
t62	PARITY<3:0>	Output valid delay		17	ns
		Output hold	2		
t63	D<63:0>	Input setup	8		ns
		Input hold	2		
t64	PARITY<3:0>	Input setup	8		ns
		Input hold	2		

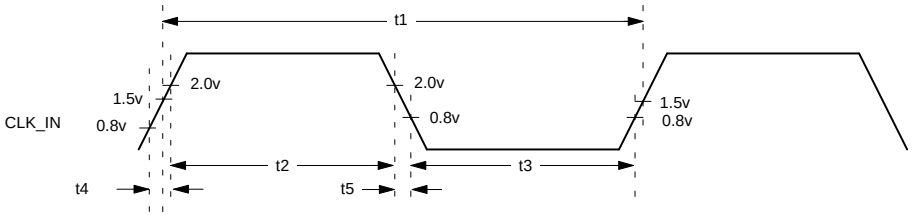
1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. Input rise and fall times are 2ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Timing specifications apply to 50MHz operating frequency in Clock Doubler Mode. (i.e. f_{CLK_IN} = 25 MHz).
5. All output timings are based on a 30pF load.

Note: –RESET, XTAL2, –ERROR, IRL<3:0>, –BMODE8, –BMODE16, CLK_ECB, –CLKDBL, –PDRESET, BIUCLOCK, all Emulator's pins, and all JTAG's pins are not listed here.

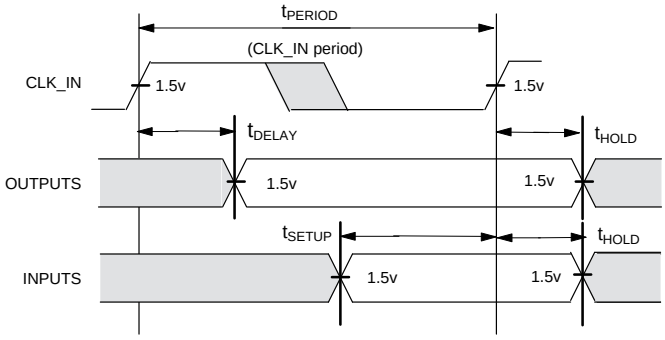


*1. CLK_IN must be stable for at least 100µs before –RESET is de-asserted.
*2. When –RESET hold time is met.

Timing 19. Reset Timing

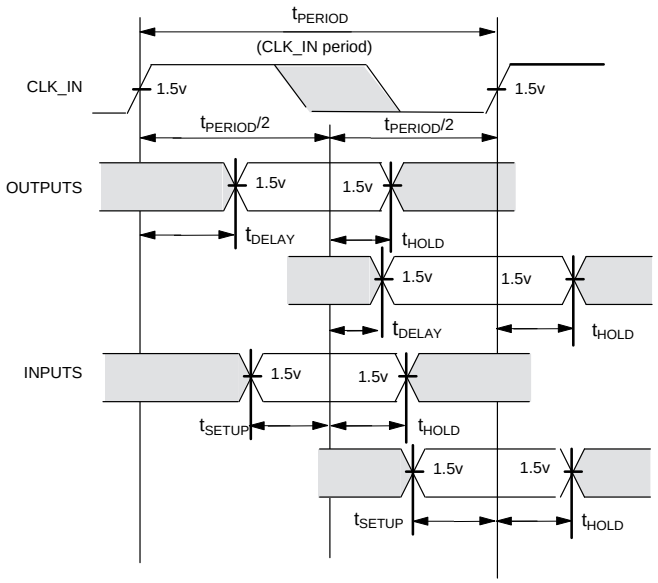


Timing 20. Clock Timing



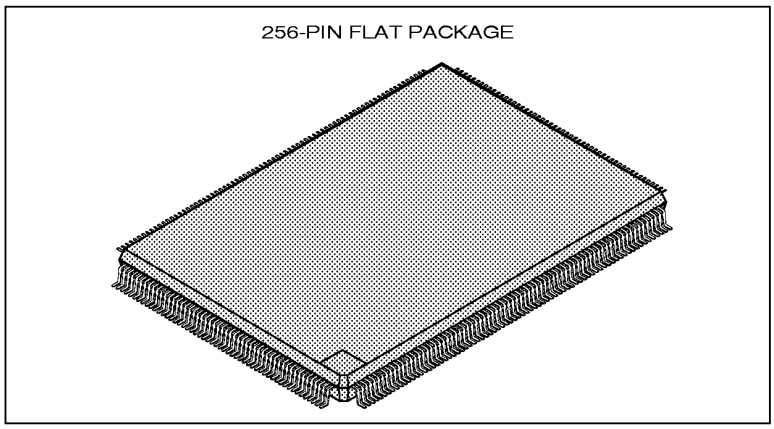
Timing 21. Output/Input Timing

Note: Setup/Delay/Hold timings are referred to the rising edge of CLK_IN (at 1.5 v point).



Timing 22. Output/Input Timing for SDRAM Interface in Clock Doubler Mode

Note: SETUP/DELAY/HOLD timings are referred to the rising edge of CLK_IN; also the midpoint of the CLK_IN period.



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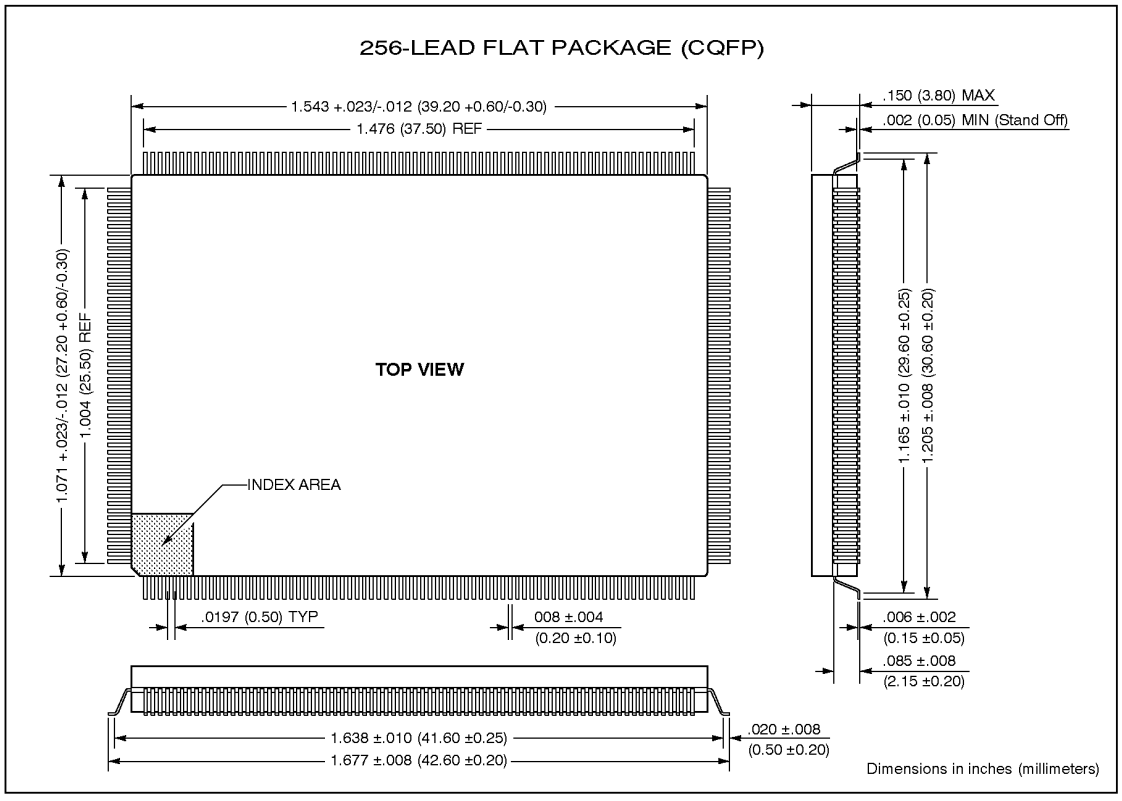

ORDERING CODE

Clock Frequency (MHz)	Ordering Code	Package Type
25/50	MB86934–25/50ZFVES	256–Pin CQFP

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