Low Cost Clock Generator for Pentium Based Designs with SDRAM Support.

Approved Product

PRODUCT FEATURES

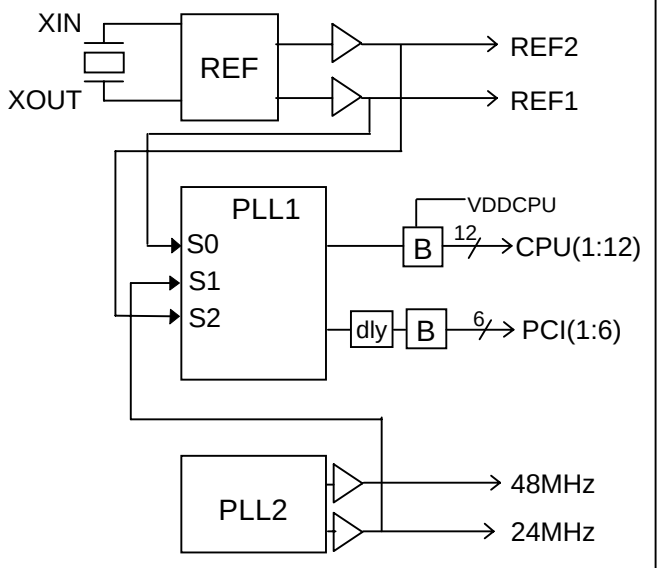
- Supports Pentium, Cyrix and AMD CPU's.
- 12 host (CPU) clocks for additional SDRAM support.
- Optional common or mixed supply mode :
  (VDD = VDDCPU = 3.3V)
  (VDD = 3.3V, VDDCPU = 2.5V)
- < 250 pS skew on CPU buffers
- < 250 pS skew on PCI buffers
- 60 mA buffer switching current
- 34 Pin SSOP package for minimum board space

FREQUENCY TABLE

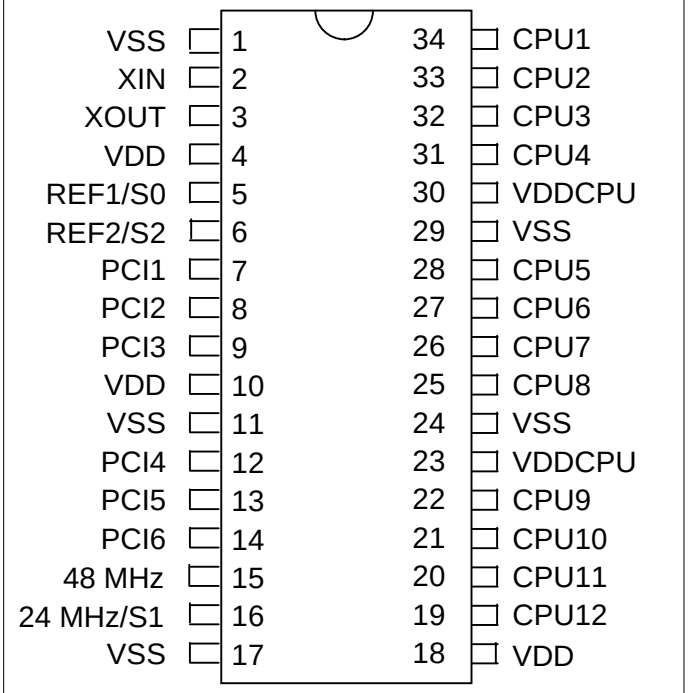
S2	S1	S0	CPU	PCI
0	0	0	tristate	tristate
0	0	1	55	a.32
0	1	0	75	a.32
0	1	1	75	37.5
1	0	0	50	25
1	0	1	55	27.6
1	1	0	60	30
1	1	1	66.6	33.3

a.32 = Asynchronous PCI.

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

CPU(1:12) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache, SDRAM, etc.. CPU1-CPU4 voltage level is controlled by VDDCPU and CPU5-CPU12 voltage level is controlled by VDDRM. All these buffers have 60 mA switching current at 3.3V.

PCI(1:6) - Low skew (<250pS) clock outputs for PCI frequencies. These buffers voltage level is controlled by VDD. All these outputs have 60 mA switching current at 3.3V.

REF1/SO - Bidirectional pin. At power up, this pin is an input frequency select line (S0). When VDD reaches its rail, the selection data is latched and this pin becomes a buffered output of on-chip reference. (see Fig.1)

REF2/S2 - Bidirectional pin. At power up, this pin is an input frequency select line (S2). When VDD reaches its rail, the selection data is latched and this pin becomes a buffered output of on-chip reference. (see Fig.1)

48MHz - Output clock for USB.

24MHz/S1 - Bidirectional pin. At power up, this pin is an input frequency select line (S1). When VDD reaches its rail, the selection data is latched and this pin becomes a buffered output for SIO clock. (see Fig.1)

VSS - Circuit common ground.
VDD - Circuit Power supply.
VDDCPU - 3.3V/2.5V logic level control for CPU(1:12) outputs.

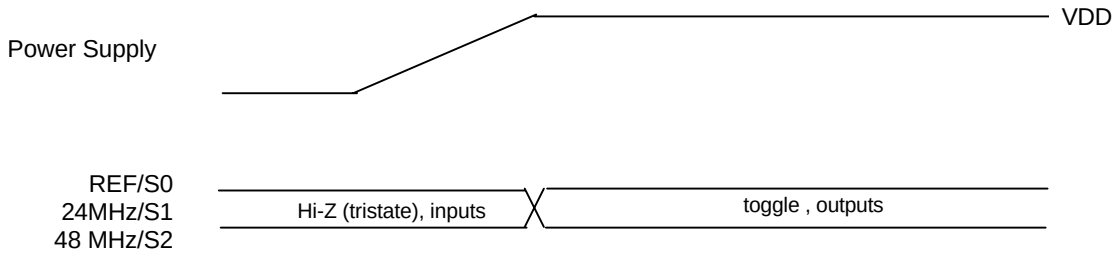

Fig.1

Low Cost Clock Generator for Pentium Based Designs with SDRAM Support.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Output Low Voltage IOL = 12mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH = 12mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State leakage Current	Ioz	-	-	10	µA	S0-S2
Dynamic Supply Current	Icc	-	-	90	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Icc (PD)	-	200	-	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDCPU = 3.3V±5%, TA = 0ºC to +70ºC

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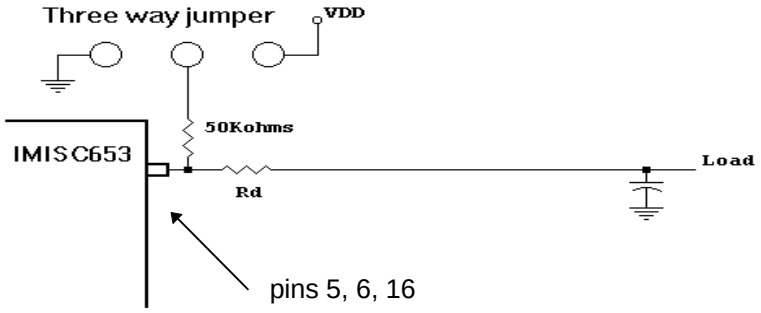
SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time	tTLH, tTHL	-	-	1.2	ns	15 pf Load CPU and PCI outputs
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI)	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
Δ Cycle-Cycles, CPU	ΔP	-	-	±250	ps	-
Jitter Absolute, CPU	tjab	-		500	ps	-
						VDD = VDDCPU = 3.3V±5%, TA = 0ºC to +70ºC

APPLICATION NOTES FOR FREQUENCY SELECTION

Pins 5, 6, and 16 are bidirectional pins and are used for selecting the output frequency of the CPU (synchronous PCI) clocks. During power-up of the SC653, these pins are in input mode, therefore, they are considered input select pins S2, S1, S0. (see Fig.1, page2). A three way Jumper with a resistor (50kΩ) method is implemented for achieving the selection as shown in Fig.2. There is no internal pullup or pulldown on any of the selection lines, therefore, it is crutial that the connection is done external to the clock generator. Inputs should not be left floating. This approach allows larger resistor values to be used (50k instead of other 10K approach), and placed close the pins before the dedamping resistor (Rd), therefore keeping the EMI levels at a minimum.



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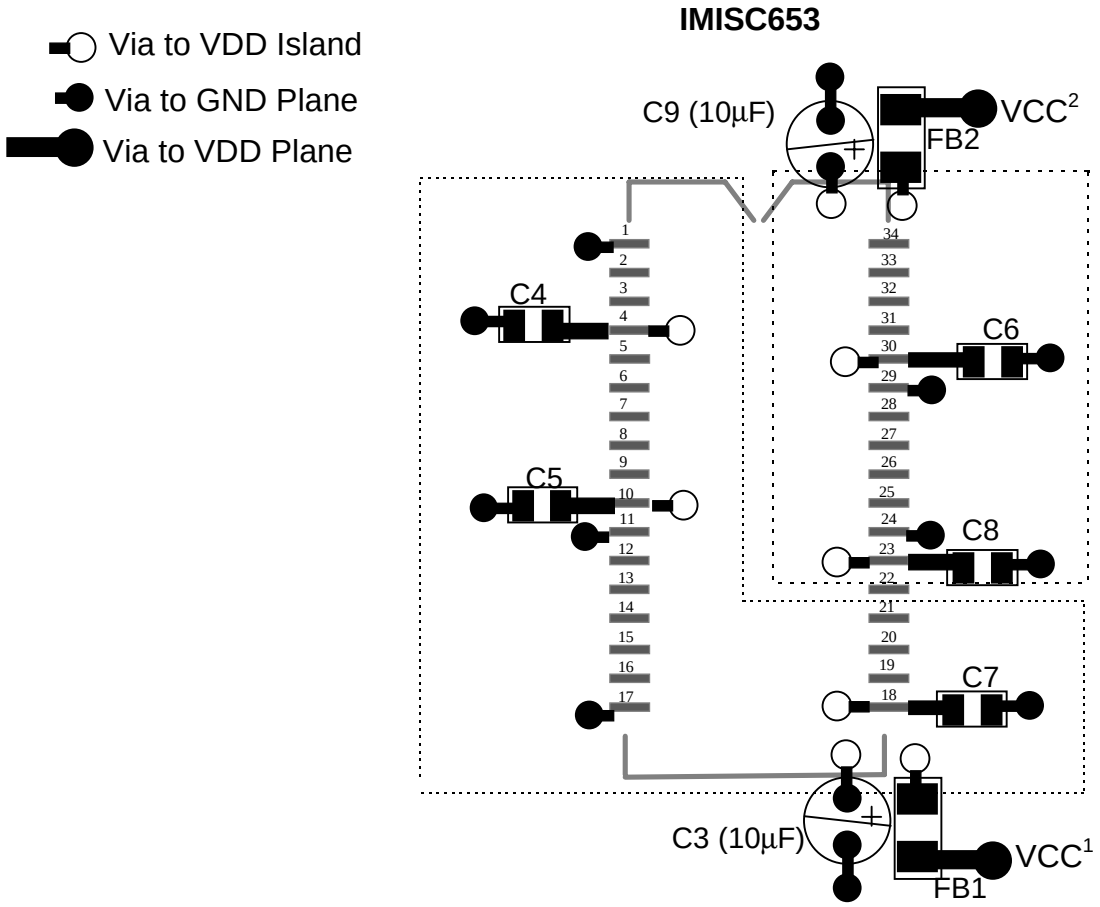
PCB LAYOUT SUGGESTION



This is only a layout recommendation for lower EMI, The designer may choose to distribute the power through traces instead of implemeting the above method of isolation through VDD islands (dashed lines). In any case, C4, C5, C6, C7, and C8 should always be used (0.1mF) and placed close to their VDD pins. The pairs of (FB1,C3) and (FB2, C9) are also used for EMI containments. The designer may choose a different approach, but at least one pair must be used.

NOTES

1. POWER SUPPLY BYPASS CAPS (O.1µF) MUST BE POSITIONED AS CLOSE AS POSSIBLE TO VDD PINS TO BE EFFECTIVE OTHER WISE THE HIGH FREQUNECY FILTERING CHARACTERISTICS OF THESE CAPS WILL BE CANCELLED OUT BY THE LEAD INDUCTANCE OF THE TRACE CONNECTING THE PIN TO THE CAP.

2. CAPACITORS MUST BE LOW LEAKAGE SUCH AS MULTILAYER CERAMIC Z5U OR X7R MATERIAL WHICH ALSO RESULTS IN LOWER IMPEDANCE AT HIGH FREQUENCY.

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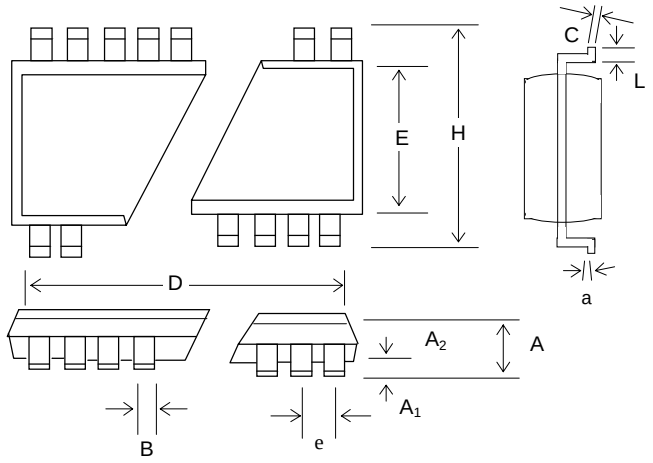
PACKAGE DRAWING AND DIMENSIONS



34 PIN SSOP OUTLINE DIMENSIONS

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.0050	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.040 BSC			1.016 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	4º	8º	0º	4º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC653DYB	34 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC653DYB
Date Code, Lot #

IMISC653DYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number