

DESCRIPTION

This family is a 4M bit dynamic RAM organized 1,048,576 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50, 60 or 70ns) and package type(SOJ, TSOP-II) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Extended data out operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Max. Active power dissipation
- JEDEC standard pinout
- 20/26-pin SOJ (300mil)
20/26-pin TSOP-II (300mil)
- Single power supply of 5V ± 10%
- Early Write or output enable controlled write
- Fast access time and cycle time

Speed	Power
50	605mW
60	495mW
70	412mW

Speed	tRAC	tCAC	tHPC
50	50ns	13ns	20ns
60	60ns	15ns	25ns
70	70ns	20ns	30ns

- Refresh cycle

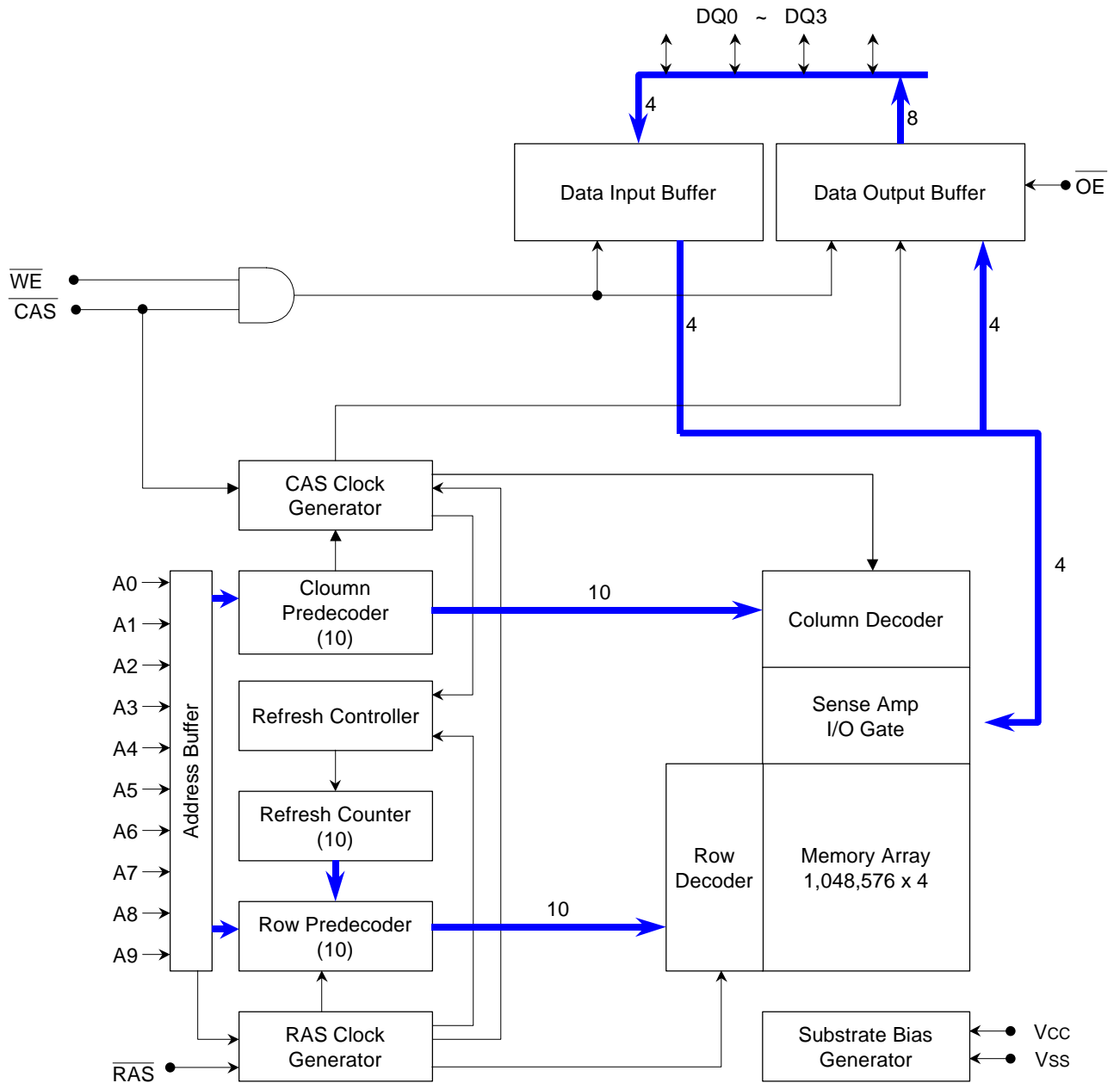
Part number	Refresh	Normal	SL-part
HY514404A	1K	16ms	128ms

ORDERING INFORMATION

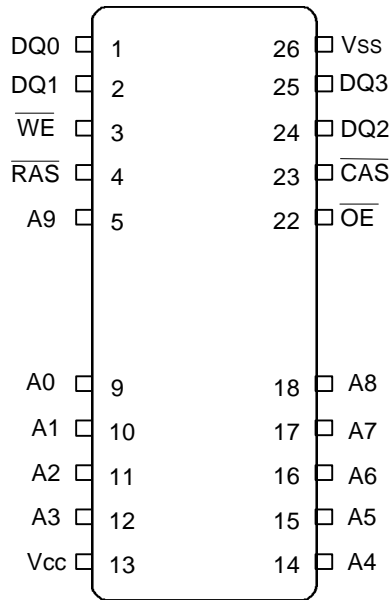
Part Name	Refresh	Power	Package
HY514404AJ	1K		20/26Pin SOJ
HY514404ALJ	1K	L-part	20/26Pin SOJ
HY514404AT	1K		20/26Pin TSOP-II
HY514404ALT	1K	L-part	20/26Pin TSOP-II

*SL : Low power with self refresh

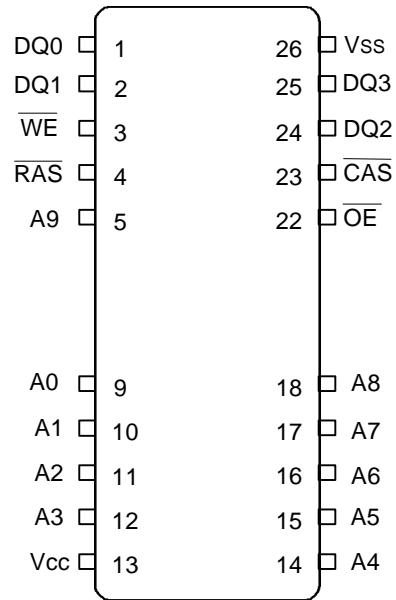
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



20/26 Pin Plastic SOJ (300mil)



20/26 Pin Plastic TSOP- II (300mil)

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A9	Address Input
DQ0~DQ3	Data In/Out
Vcc	Power (5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature	0 to 70	°C
T _{STG}	Storage Temperature	-55 to 150	°C
V _{IN} , V _{OUT}	Voltage on Any Pin relative to V _{SS}	-1.0 to 7.0	V
V _{CC}	Voltage on V _{CC} relative to V _{SS}	-1.0 to 7.0	V
I _{OS}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	0.9	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I _{LI}	Input Leakage Current (Any input)	V _{SS} ≤ V _{IN} ≤ V _{CC} + 1.0 All other pins not under test = V _{SS}	-10	10	μA
I _{LO}	Output Leakage Current (Any input)	V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH}	-10	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -5.0mA	2.4	-	V

DC CHARACTERISTICS

(TA = 0°C to 70°C , VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max.	Unit
Icc1	Operating Current	/RAS, /CAS Cycling tRC = tRC(min)	50 60 70	100 90 75	mA
Icc2	TTL Standby Current	/RAS, /CAS ≥ VIH(min) Other inputs ≥ VSS		2	mA
Icc3	/RAS-only Refresh Current	/RAS Cycling, /CAS = VIH tRC = tRC(min)	50 60 70	110 90 75	mA
Icc4	EDO mode Current	/CAS Cycling, /RAS = VIL tHPC = tHPC(min)	50 60 70	115 90 75	mA
Icc5	CMOS Standby Current	/RAS = /CAS ≥ VCC - 0.2V	SL-part	1 200	mA μA
Icc6	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V tRC = tRC(min.)	50 60 70	95 80 65	mA
Icc7	Battery Back-up Current (L-part)	tRC=125μs /CAS = CBR cycling or 0.2V /OE & /WE = VCC - 0.2V Address = VCC-0.2V or 0.2V DQ0~DQ9 = VCC-0.2, 0.2V or Open	tRAS ≤ 300ns	300	μA
			tRAS E 1μs	400	

Note

- Icc1, Icc3, Icc4, Icc6 and Icc6 depend on output loading and cycle rates(tRC and tHPC).
- Specified values are obtained with output unloaded.
- Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=VIH within one EDO mode cycle time tHPC.
- Only tRAS(max) = 1μs is applied to refresh of battery backup but tRAS(max) = 10μs is to applied to normal functional operation.
- Icc5(max.), Icc7 are applied to L-part only.

AC CHARACTERISTICS

(TA = 0 °C to 70 °C, VCC = 5V ± 10% , VSS = 0V, unless otherwise noted.)

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tRC	Random read or write cycle time	85	-	105	-	125	-	ns	
tRWC	Read-modify-write cycle time	120	-	142	-	167	-	ns	
tHPC	EDO mode cycle time	20	-	25	-	30	-	ns	
tHPRWC	EDO mode read-modify-write cycle time	62	-	73	-	85	-	ns	
tRAC	Access time from /RAS	-	50	-	60	-	70	ns	4,9,10
tCAC	Access time from /CAS	-	13	-	15	-	20	ns	4,9
tAA	Access time from column address	-	25	-	30	-	35	ns	4,10
tCPA	Access time from /CAS precharge	-	30	-	35	-	35	ns	4,15
tCLZ	/CAS to output low impedance	0	-	0	-	0	-	ns	4
tT	Transition time(rise and fall)	2.5	50	2.5	50	2.5	50	ns	3
tRP	/RAS precharge time	30	-	40	-	50	-	ns	
tRAS	/RAS pulse width	50	10K	60	10K	70	10K	ns	
tRASP	/RAS pulse width(EDO mode)	50	100K	60	100K	70	100K	ns	
tRSH	/RAS hold time	13	-	15	-	13	-	ns	
tCSH	/CAS hold time	40	-	40	-	50	-	ns	
tCAS	/CAS pulse width	8	10K	10	10K	15	10K	ns	
tRCD	/RAS to /CAS delay time	20	37	20	45	20	50	ns	9
tRAD	/RAS to column address delay time	15	25	15	30	15	35	ns	10
tCRP	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	15
tCP	/CAS precharge time	7	-	10	-	10	-	ns	17
tASR	Row address set-up time	0	-	0	-	0	-	ns	
tRAH	Row address hold time	10	-	10	-	10	-	ns	
tASC	Column address set-up time	0	-	0	-	0	-	ns	14
tCAH	Column address hold time	8	-	10	-	15	-	ns	14
tRAL	Column address to /RAS lead time	25	-	30	-	35	-	ns	
tRCS	Read command set-up time	0	-	0	-	0	-	ns	14
tRCH	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	6,14
tRRH	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	6
tWCH	Write command hold time	8	-	10	-	15	-	ns	14
tWP	Write command pulse width	10	-	10	-	10	-	ns	
tRWL	Write command to /RAS lead time	13	-	15	-	15	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tcWL	Write command to /CAS lead time	8	-	10	-	15	-	ns	16
tDS	Data-in set-up time	0	-	0	-	0	-	ns	7
tDH	Data-in hold time	8	-	10	-	15	-	ns	7
tREF	Refresh period(1024 cycles)	16	-	16	-	16	-	ms	12
	Refresh period(L-part)	128	-	128	-	128	-	ms	11
twCS	Write command set-up time	0	-	0	-	0	-	ns	8,14
tcWD	/CAS to /WE delay time	33	-	37	-	45	-	ns	8
trWD	/RAS to /WE delay time	70	-	80	-	95	-	ns	8
tAWD	Column address to /WE delay time	45	-	50	-	60	-	ns	8
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	14
tCHR	/CAS hold time(CBR cycle)	10	-	10	-	10	-	ns	15
trPC	/RAS to /CAS precharge time	5	-	5	-	5	-	ns	14
tcPT	/CAS precharge time(CBR counter test)	25	-	30	-	35	-	ns	17
tROH	/RAS hold time referenced to /OE	10	-	10	-	10	-	ns	
toEA	/OE access time	-	13	-	15	-	20	ns	
toED	/OE to data delay	13	-	15	-	20	-	ns	
toEZ	Output buffer turn-off delay time from /OE	0	13	0	15	0	15	ns	5
toEH	/OE command hold time	13	-	15	-	20	-	ns	
tcPWD	/WE delay time from /CAS precharge	50	-	55	-	65	-	ns	8
trHCP	/RAS hold time from /CAS precharge	30	-	35	-	40	-	ns	
tWRP	/WE to /RAS Precharge time (CBR Cycle)	10	-	10	-	10	-	ns	
tWRH	/WE to /RAS Hold time(CBR Cycle)	10	-	10	-	10	-	ns	
trPS	/RAS Precharge Time	85	-	105	-	125	-	ns	
tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
treZ	Output Buffer Turn Off Delay Time from /RAS	0	13	0	15	0	15	ns	
twez	Output Buffer Turn Off Delay Time from /WE	3	13	0	15	0	15	ns	
toEP	/OE Pulse Width	10	-	10	-	10	-	ns	
toCH	/OE to /CAS Hold Time	0	-	0	-	0	-	ns	
tCHO	/CAS Hold Time to /OE	5	-	5	-	7	-	ns	
twED	/WE to Data Delay Time	13	-	15	-	15	-	ns	
twPE	/WE Pulse Width for Output Dsiable when /CASS High	10	-	10	-	10	-	ns	

NOTE

1. An initial pause of 200 μ s is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up, the HY514404A could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid VIH in other to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. tCEZ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS \geq tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD \geq tRWD(min.), tCWD \geq tCWD(min.), tAWD \geq tAWD(min), and tCPWD \geq tCPWD(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=128ms is applied to L-parts only.
12. A burst of 1024 CBR refresh cycles must be executed within 16ms (128ms for SL-part) after exiting self refresh.
13. When CAS goes low at the same time, 4bits data are written into the device.
14. These parameters are determined by the earlier falling edge of /CAS.
15. These parameters are determined by the later rising edge of /CAS.
16. tCWL must be satisfied by /CAS for 4bits access cycle.
17. tCP and tCPT are measured when /CAS and is high state.

CAPACITANCE

(TA = 25°C, Vcc = 5V \pm 10%, Vss = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
CIN1	Input Capacitance (A0~A8)	-	5	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
CDQ	Data Input / Output Capacitance (DQ0~DQ3)	-	7	pF