The Discovery™ GT-64260 provides a breakthrough in PowerPC®-based communications systems architecture, setting a new standard for performance and integration.
Marvell provides advanced LAN/MAN/WAN silicon solutions for leading-edge networking applications throughout the converged network.

Marvell's highly integrated communications systems on silicon simplifies designs, reduces development risks and costs, and substantially improves time-to-market for manufacturers of data communications and telecommunications equipment. Marvell's semiconductor chips are highly-integrated, scalable, programmable, and flexible to meet the demands of technologically sophisticated network applications.

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The Industry’s Most Powerful System Controller

Innovative Architecture and High-Speed Interfaces Deliver Superior Performance

The Discovery™ GT-64260 supports industry standard PowerPC® processors, including Motorola MPC74XX and IBM 750 series processors. Both 60x and advanced MPX bus protocols are supported. An on-chip SDRAM memory controller with a 72-bit wide (64-bit with 8-bit ECC), 100 MHz interface enables high speed data transactions between memory, processor and PCI peripherals.

Advanced Crossbar Fabric

The Discovery GT-64260 architecture employs a high-speed crossbar fabric to enable non-blocking concurrent transactions between the CPU, PCI, LAN, WAN, and memory, greatly enhancing overall system performance. The internal crossbar fabric provides an aggregate throughput of 76 Gbps to deliver unprecedented performance for next-generation communications equipment.

High Integration Reduces Design Time and Board Space Requirements

The Discovery GT-64260 integrates system peripherals necessary to build a high performance PowerPC system: PCI bridge and arbiter, interrupt controller, eight channel DMA engine, I²C controller, timers, multi-channel device bus interface, and a 72-bit SDRAM memory controller. In addition, three 10/100 Ethernet controllers and two Multi-Protocol Serial Controllers (MPSCs) are integrated for communications applications. The MPSCs can be used as UARTs if needed.

Ideal for Communications Applications

Three 10/100 Mbps full-duplex Ethernet ports on the Discovery GT-64260 are fully compliant with IEEE 802.3/802.3u
The GT-64260 has Quality of Service (QoS) features to enable flow classification based on packet content. Each GT-64260 Ethernet MAC includes two transmit and four receive priority queues. Data can be queued based on MAC addresses, 802.1p tags or IP header Type of Service (ToS) fields. As the packet classification is done in hardware by the GT-64260 at the MAC level, CPU processing bandwidth is saved for other critical application functions.

The GT-64260 supports several packet-based WAN interfaces including ISDN, frame relay, unchannelized T1/T3, xDSL (HDSL2, SDSL), HSSI, and more. Two on-chip MPSCs support UART, HDLC, BISYNC, and Transparent protocols, and can be configured as simple debug/console ports if needed.

Flexible PCI Architecture

The Discovery GT-64260 can be configured to support two independent 64-bit/32-bit PCI interfaces. Each PCI interface can operate at up to 66 MHz with zero wait states. The PCI units can act either as a master, initiating a PCI-bus transaction or as a slave, responding to PCI-bus transactions. The PCI-to-PCI transaction bridging and PCI arbitration logic are integrated to optimize system performance and simplify board design.

Integrated Crossbar Maximizes System Bandwidth

The Discovery™ GT-64260 chip combines an advanced high-performance crossbar architecture with Marvell’s market-leading system controller technology to deliver unprecedented performance. With an aggregate throughput of 76 Gbps, the GT-64260’s crossbar fabric supports non-blocking concurrent transactions among peripherals at full bus speeds.

Discovery EV-64260

Development Platform

- System-level development platform supporting the Motorola MPC74XX/MP750 and IBM 750 PowerPC CPUs
- Wind River VxWorks® Board Support Package available
- Four 32/64-bit PCI expansion board slots
- Three 10/100 Mbps Ethernet ports
- Two serial ports (UART, LVDS, and V.35 PHY modules available)
- Supports 72-bit SDRAM DIMMs (up to 2 GB)
**High Integration Reduces Design Time**

**DISCOVERY™ GT-64260 BLOCK DIAGRAM**

- **PowerPC CPU**
- **SDRAM**
- **PCI 0**
- **10/100 MAC**
- **Crossbar Fabric**
- **Device**
- **I2C**
- **DMA**
- **GPIO**
- **MPSC 0 (55 Mbps)**
- **MPSC 1 (55 Mbps)**
- **10/100 MAC**
- **PCI 1**
- **PCI 0**

**Feature Highlights:**

- **Discovery™ GT-64260 Features**
  - High-Performance 64-Bit PowerPC CPU Interface
  - 64-Bit SDRAM Controller
  - Integrated System Peripherals
  - Eight Independent Direct Memory Access (IDMA) Channels
  - Three 10/100 Mbps Fast Ethernet MACs
  - Two Multi-Protocol Serial Controllers
  - Dual 32/64-Bit, 66 MHz PCI 2.2 Interfaces
  - Supports Full-Duplex OC-48 Data Rates

**Discovery Development Platform**

- 100 MHz 64-bit
- 32-bit, 100 MHz
- 64-bit, 100 MHz
- 64-bit, 66 MHz
High-Performance Controller for PowerPC-Based Communications Systems
- 64-bit 100 MHz CPU bus interface
- 72-bit (64-bit with 8-bit ECC) 100 MHz SDRAM controller
- Dual 32/64-bit 66 MHz PCI interfaces
- Advanced internal crossbar fabric
- 32-bit 100 MHz peripheral device bus interface

Integrated Systems Peripherals
- Interrupt controller
- 8 channel DMA controller
- Device bus controller
- PCI arbiter
- Master/slave I2C controller
- SDRAM controller
- Timers

Advanced Communications Unit
- Three 10/100 Ethernet controllers with packet filtering and priority queuing
- Two Multi-Protocol Serial Controllers (MPSCs)

64-Bit PowerPC CPU Bus Interface
- Motorola MPC603e, MPC750, MPC8260, MPC74XX and IBM 750/750CX processor support
- 60X and advanced MPX bus protocols supported
- 100 MHz CPU bus frequency (2.5V or 3.3V configuration)
- Configurable cache coherency
- Supports splitread transactions with out-of-order completion

High-Performance SDRAM Controller
- 100 MHz memory interface
- 4 GB address space
- Supports 2-way and 4-way bank interleaving
- Supports up to 16 open pages

Data Integrity Support Between CPU, PCI and DRAM Interfaces
- ECC on 64-bit wide SDRAM
- Parity support on CPU and PCI buses
- Full error reporting including error counters

32/64-Bit, 66 MHz PCI 2.2 Interface
- Dual PCI interface
- 32 or 64-Bit, 66 MHz PCI interface
- Transaction bridging between PCI interfaces
- Supports PCI delayed read transactions

Advanced 0.18u Process
- 1.8V core
- 2.5V/3.3V CPU interface
- 3.3V I/O
- 5V tolerant PCI interface
- 100 MHz speed

665 PBGA Package
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