EN29F002 / EN29F002N
2 Megabit (256K x 8-bit) Flash Memory

FEATURES

- 5.0V ± 10% for both read/write operation
- Read Access Time
  - 45ns, 55ns, 70ns, and 90ns
- Fast Read Access Time
  - 70ns with C_{load} = 100pF
  - 45ns, 55ns with C_{load} = 30pF
- Block Architecture:
  One 16K byte Boot Block, Two 8K byte Parameter Blocks, one 32K byte and three 64K byte main Blocks
- Boot Block Top/Bottom Programming Architecture
- High performance program/erase speed
  - Byte program time: 10µs typical
  - Block erase time: 500ms typical
  - Chip erase time: 3.5s typical
- Low Standby Current
  - 1µA CMOS standby current-typical
  - 1mA TTL standby current
- Low Power Active Current
  - 30mA active read current
  - 30mA program/erase current
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Hardware $\overline{\text{RESET}}$ Pin (n/a for EN29F002N)
- Single Block and Chip Erase
- Block Protection / Temporary Block Unprotect ($\overline{\text{RESET}}$ = Vpp)
- Block Unprotect Mode
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes:
  Read and program another block during Erase Suspend Mode
- 0.4 µm double-metal double-poly triple-well CMOS Flash Technology
- Latch-Up ≥ 200mA
- Low Vcc write inhibit ≤ 3.2V
- 100K endurance cycle
- Package Options
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
- Commercial and Industrial Temperature Ranges

GENERAL DESCRIPTION

The EN29F002 / EN29F002N is a 2-Megabit, electrically erasable, read/write non-volatile flash memory. Organized into 256K words with 8 bits per word, the 2M of memory is arranged in seven blocks (with top/bottom configuration), including one 16K Byte Boot Block, two 8K Byte Parameter blocks, and four main blocks (one 32K Byte and three 64K Byte). Any byte can be programmed typically at 10µs. The EN29F002 / EN29F002N features 5.0V voltage read and write operation. The access times is as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29F002 / EN29F002N has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls which eliminate bus contention issues. This device is designed to allow either single(or multiple) block or full chip erase operation, where each block can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each block.

TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A17	Addresses
DQ0-DQ7	Data Input/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$ (n/a for EN29F002N)	Hardware Reset Block Unprotect
Vcc	Supply Voltage (5V ± 10%)
Vss	Ground

FIGURE 1. LOGIC DIAGRAM

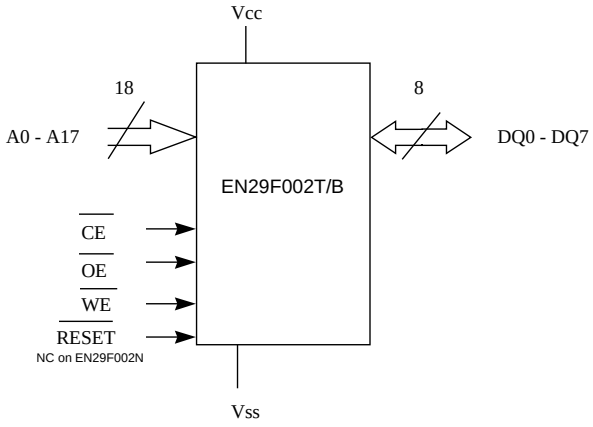


TABLE 2. BLOCK ARCHITECTURE

TOP BOOT BLOCK

BLOCK	ADDRESSES	SIZE (Kbytes)
6	3C000h - 3FFFFh	16
5	3A000h - 3BFFFh	8
4	38000h - 39FFFh	8
3	30000h - 37FFFh	32
2	20000h - 2FFFFh	64
1	10000h - 1FFFFh	64
0	00000h - 0FFFFh	64

BOTTOM BOOT BLOCK

ADDRESSES	SIZE (Kbytes)
30000h - 3FFFFh	64
20000h - 2FFFFh	64
10000h - 1FFFFh	64
08000h - 0FFFFh	32
06000h - 07FFFh	8
04000h - 05FFFh	8
00000h - 03FFFh	16

BLOCK DIAGRAM

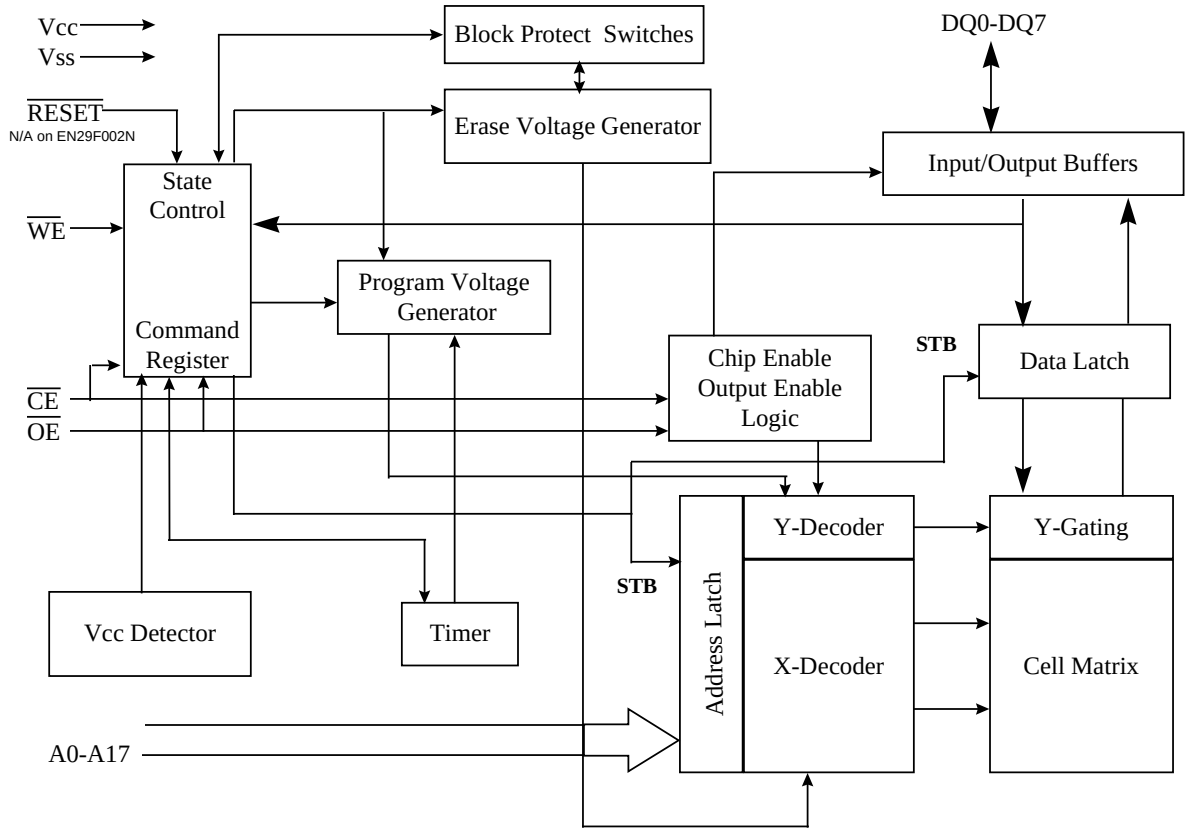


FIGURE 2. PDIP

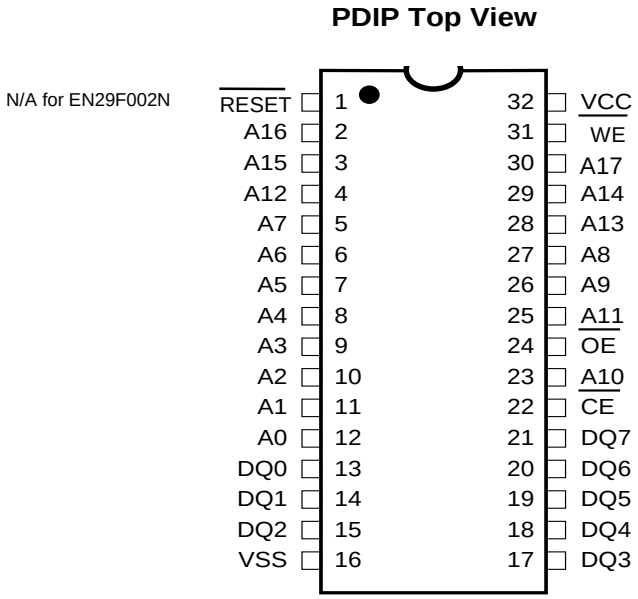


FIGURE 3. TSOP

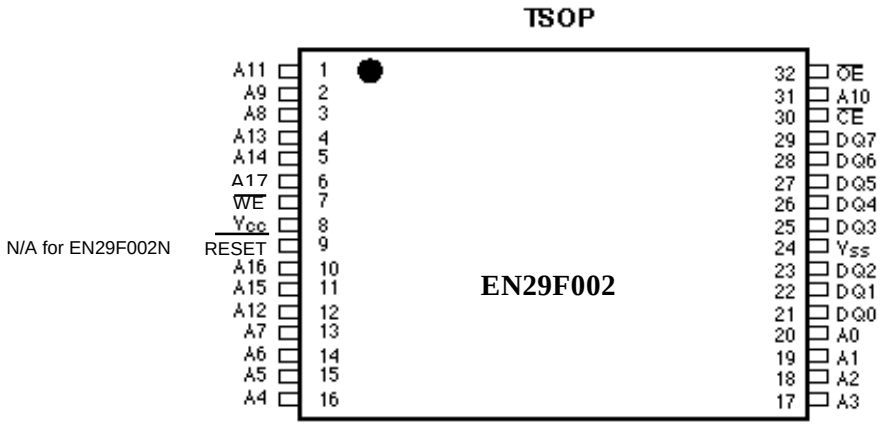


FIGURE 4. PLCC

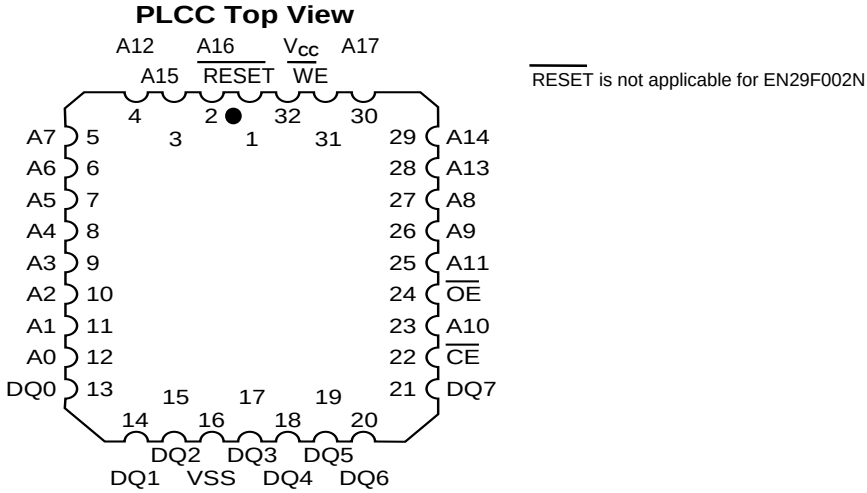


TABLE 3. OPERATING MODES

2M FLASH USER MODE TABLE

	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{RESET}$	A9	A8	A6	A1	A0	Ax/y	DQ(0-7)
USER MODE											
$\overline{RESET}$ (n/a for EN29F002N)	X	X	X	L	X	X	X	X	X	X	HI-Z
STANDBY	H	X	X	H	X	X	X	X	X	X	HI-Z
READ	L	H	L	H	A9	A8	A6	A1	A0	Ax/y	DQ(0-7)
OUTPUT DISABLE	L	H	H	H	A9	A8	A6	A1	A0	Ax/y	HI-Z
READ MANUFACTURE ID	L	H	L	H	VID	L/H	L	L	L	X	MANUFACTURE ID
READ DEVICE ID	L	H	L	H	VID	L/H	L	L	H	X	DEVICE ID(T/B)
VERIFY BLOCK PROTECT	L	H	L	H	VID	X	L	H	L	X	CODE
ENABLE BLOCK PROTECT	L	L	VID	H	VID	X	L	X	X	X	X
BLOCK UNPROTECT	L	L	VID	H	VID	X	H	H	L	X	X
WRITE	L	L	H	H	A9	A8	A6	A1	A0	Ax/y	DIN(0-7)
TEMPORARY BLOCK UNPROTECT	X	X	X	VID	X	X	X	X	X	X	X

NOTES:
1) L = V_{IL}, H = V_{IH}, V_{ID} = 12.0V ± 0.5V
2) X = Either V_{IH} or V_{IL}

TABLE 4. DEVICE IDENTIFICTION

2M FLASH MANUFACTURER/DEVICE ID TABLE

	A8	A6	A1	A0	DQ(7-0) HEX
READ MANUFACTURER ID	L	L	L	L	MANUFACTURER ID 7F
READ MANUFACTURER ID	H	L	L	L	MANUFACTURER ID 1C
READ DEVICE ID (Top Architecture)	L	L	L	H	DEVICE ID 7F
READ DEVICE ID (Top Architecture)	H	L	L	H	DEVICE ID 92
READ DEVICE ID (Bottom Architecture)	L	L	L	H	DEVICE ID 7F
READ DEVICE ID (Bottom Architecture)	H	L	L	H	DEVICE ID 97

USER MODE DEFINITIONS

Reset Mode

EN29F002 features a Reset mode that resets the program and erase operation immediately to read mode. If reset ($\overline{RESET}$ = L) is executed when program or erase operation were in progress, the program or erase which was terminated should be repeated since data will be corrupted. This mode is not available for EN29F002N.

Standby Mode

The EN29F002 / EN29F002N has a CMOS-compatible standby mode which reduces the current to < 1µA (typical). It is placed in CMOS-compatible standby when $\overline{CE}$ and the $\overline{RESET}$ pins are at $V_{CC} \pm 0.5$ V ($\overline{CE}$ pin only, for EN29F002N). The device also has a TTL-compatible standby mode which reduces the maximum V_{CC} current to < 1mA. It is placed in TTL-compatible standby when $\overline{CE}$ and $\overline{RESET}$ pins are at V_{IH}. Another method of entering standby mode uses only the $\overline{RESET}$ pin (n/a for EN29F002N). When $\overline{RESET}$ pin is at $V_{SS} \pm 0.3$V, the device enters CMOS-compatible standby with current typically reduced to < 1 µA. When $\overline{RESET}$ pin is at V_{IL}, the device enters TTL-compatible standby with current reduced to < 1mA. When in standby modes, the outputs are in a high-impedance state independent of the $\overline{OE}$ input.

Read Mode

The EN29F002 / EN29F002N has two control functions which must be satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Read is selected when both $\overline{CE}$ and $\overline{OE}$ pins are held at V_{IL} with the $\overline{WE}$ pin held at V_{IH}. Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. Assuming that addresses are stable, chip enable access time (t_{CE}) is equal to the delay from stable $\overline{CE}$ to valid data at output pins. Data is available at the outputs after output enable access time (t_{OE}) from the falling edge of $\overline{OE}$, assuming the $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Output Disable Mode

When the $\overline{OE}$ pin is at a logic high level (V_{IH}), the output from the EN29F002 / EN29F002N is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The manufacturer and device type can be identified by hardware or software operations. This mode allows applications or programming equipment automatically matching the device with its corresponding interface characteristics.

To activate the Auto Select Identification mode, the programming equipment must force 12.0 V ± 0.5V on address line A9 of the EN29F002T/B. Two identifier bytes can then be sequenced from the device outputs by toggling address lines A0 and A8 from V_{IL} to V_{IH}.

The manufacturer and device identification may also be read via the command register. By following the command sequence referenced in the Command Definition Table (Table 5). This method is desirable for in-system identification (using only + 5.0V).

When A0 = A1 = A6 = V_{IL} and by toggling A8 from V_{IL} to $V_{IH,}$ the Manufacturer ID can be read as Eon = 7F, 1C (hex) to identify EON . When A0 = V_{IH}, A1 = A6 = $V_{IL,}$ and by toggling A8 from V_{IL} to V_{IH}, the Device Code can be read as 7F, 92 (hex) for EN29F002T or as 7F, 97 (hex) for EN29F002B (See

Table 4). All identifiers for manufacturer and device codes possess odd parity with the DQ7 defined as the parity bit.

Write Mode

Write is used for device programming and erase through the command register. This mode is selected with $\overline{CE}$ = $\overline{WE}$ = L and $\overline{OE}$ = H. The contents of the command register are the inputs to the internal state machine. The command register is a set of latches used to store the commands along with the addresses and data information needed to execute that command. Address latching occurs on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs later) and data latching occurs on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs first).

Temporary Block Unprotect Mode

EN29F002 allows protected blocks to be temporarily unprotected for making changes to data stored in a protected block in system (n/a for EN29F002N). To activate the temporary block unprotect, the $\overline{RESET}$ pin must be set to a high voltage (+ 12V). In this mode, protected blocks can be programmed or erased by selecting the block addresses. Once the high voltage (+ 12V) is removed from $\overline{RESET}$ pin, all previously protected blocks will revert to their protected state.

$\overline{RESET}$ Hardware Reset Mode (not available on EN29F002N)

Resetting the EN29F002 device is performed when the $\overline{RESET}$ pin is set to V_{IL} and kept low for at least 500ns. The internal state machine will be reset to the read mode. Any program/erase operation in progress during hardware reset will be terminated and data may be corrupted.
If the $\overline{RESET}$ pin is tied to the system reset command, the device will be automatically reset to the read mode and enable the system's microprocessor to read the boot-up firmware from the FLASH memory.

COMMAND DEFINITIONS

The operations of the EN29F002 are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Block Protection, Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to the read mode.

Table 5. EN29F002 Command Definitions

Command Sequence Read/Reset	Write Cycles Req'd	1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Write Cycle		5th Write Cycle		6th Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXh	F0h	RA	RD								
Read/Reset	4	555h	AAh	AAAh	55h	555h	F0h	RA	RD				
AutoSelect Manufacturer ID	4	555h	AAh	AAAh	55h	555h	90h	000h/ 100h	7Fh/ 1Ch				
AutoSelect Device ID (Top Boot)	4	555h	AAh	AAAh	55h	555h	90h	001h/ 101h	7Fh/ 92h				
AutoSelect Device ID (Bottom Boot)	4	555h	AAh	AAAh	55h	555h	90h	001h/ 101h	7Fh/ 97h				
AutoSelect Block Protect Verify	4	555h	AAh	AAAh	55h	555h	90h	BA & 02h	00h/ 01h				
Byte Program	4	555h	AAh	AAAh	55h	555h	A0h	PA	PD				
Chip Erase	6	555h	AAh	AAAh	55h	555h	80h	555h	AAh	AAAh	55h	555h	10h
Block Erase	6	555h	AAh	AAAh	55h	555h	80h	555h	AAh	AAAh	55h	BA	30h
Block Erase Suspend	1	xxxh	B0h										
Block Erase Resume	1	xxxh	30h										

Notes:

RA = Read Address: address of the memory location to be read
RD = Read Data: data read from location RA during Read operation
PA = Program Address: address of the memory location to be programmed
PD = Program Data: data to be programmed at location PA
BA = Block Address: address of the block to be erased. Address bits A17-A13 uniquely select any block.

Byte Programming Command

Programming the EN29F002 is performed on a byte-by-byte basis using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. The program operation is terminated automatically by an internal timer. Address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The program operation is completed when EN29F002 returns the equivalent data to the programmed location.

Programming status may be checked by sampling data on DQ7 ($\overline{DATA}$ polling) or on DQ6 (toggle bit). Changing data from 0 to 1 requires an erase operation. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

EN29F002 ignores commands written during Byte Programming. If a hardware $\overline{RESET}$ occurs during Byte Programming, data at the programmed location may get corrupted. Programming is allowed in any sequence and across any block boundary.

Chip Erase Command

An auto Chip Erase algorithm is employed when the Chip Erase command sequence is performed. Although the Chip Erase command requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles and the chip erase command, the user is responsible for writing only the Erase Setup command and the Erase command. The Erase Setup command is

performed by writing 30H to the Command Register. The Auto Chip Erase algorithm automatically programs and verifies the entire memory array for an all "0" pattern prior to the erase. The Chip Erase Command is performed by again writing 10H to the command register. The EN29F002 will automatically time the erase pulse width, verify the erase, return the sequence count, provide a erase status through $\overline{DATA}$ POLLING (when data on DQ7 is "1"), and returns to the READ mode after completion of Chip Erase.

Block Erase Command

Block Erase requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles, and the Block Erase command. Any block may be erased by latching any address within the desired block on the falling edge of $\overline{WE}$ while the Erase Command (30H) is latched on the rising edge of $\overline{WE}$. Block Erase will commence after an 80μs time-out window.

Any command other than Block Erase or Erase Suspend during this time-out period will reset the device to the read mode, without completing the Block Erase command sequence.

The EN29F002 device automatically programs and verifies all memory locations in the selected block for an all "0" pattern prior to the erase. Unselected blocks are unaffected by the Block Erase command. The EN29F002 requires no timing signals during block erase. Erase is completed when data on DQ7 becomes "1", and the device returns to the READ mode after completion of Block Erase.

Erase Suspend / Resume Command

Erase suspend allows interruption of block erase operations to perform data reads from block not being erased. Erase suspend applies only to Block Erase operations including the time-out period. Writing an Erase Suspend command during Block Erase Timeout results in an immediate termination of the time-out period and suspension of erase operation.

EN29F002 ignores any commands during erase suspend other than the $\overline{RESET}$ (n/a for EN29F002N) or Erase Resume commands. Writing erase resume continues erase operations. Addresses are DON'T CARE when writing Erase Suspend or Erase Resume commands.

EN29F002 takes 0.1 - 15 μs to suspend erase operations after receiving Erase Suspend command. Check completion of erase suspend by polling DQ7 and/or DQ6. EN29F002 ignores redundant writes of erase suspend.

EN29F0002 defaults to erase-suspend-read mode while an erase operation has been suspended. While in erase-suspend-read mode, EN29F002 allows reading data in any block not undergoing block erase, which is treated as standard read mode.

Write the Resume command 30h to continue operation of Block erase. En29F002 ignores redundant writes of the Resume command. En29F002 permits multiple suspend/resume operations during block erase.

Block Protect

The hardware block or sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operation in previously protected sectors.

Block protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. See **Data Protection** or contact Eon Silicon Devices, Inc. for an additional supplement on this feature.

WRITE OPERATION STATUS

DQ7
$\overline{\text{DATA}}$ Polling

The EN29F002 provides $\overline{\text{DATA}}$ Polling on DQ7 to indicate to the host system the status of the embedded operations. The $\overline{\text{DATA}}$ Polling feature is active during the Byte Programming, Block Erase, Chip Erase, Erase Suspend and block erase time-out window. (See Table 6)

When the Byte Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the Byte Programming, an attempt to read the device will produce the true data last written to DQ7. For the Byte Programming, $\overline{\text{DATA}}$ polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a "0" at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the "1" at the DQ7 output during the read. For Chip Erase, the $\overline{\text{DATA}}$ polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the six-cycle sequence. For Block Erase, $\overline{\text{DATA}}$ polling is valid after the last rising edge of the block erase $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse.

$\overline{\text{DATA}}$ Polling must be performed at any address within a block that is being programmed or erased and not a protected block. Otherwise, $\overline{\text{DATA}}$ polling may give an inaccurate result if the address used is in a protected block.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable ($\overline{\text{OE}}$) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for $\overline{\text{DATA}}$ Polling (DQ7) is shown on Flowchart 5. The $\overline{\text{DATA}}$ Polling (DQ7) timing diagram is shown in Figure 8.

DQ6
Toggle Bit

The EN29F002 provides a "Toggle Bit" on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by toggling $\overline{\text{OE}}$ or $\overline{\text{CE}}$) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is complete, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Byte Programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four-cycle sequence. For Chip Erase, the Toggle Bit is valid after the rising edge of the sixth-cycle sequence. For Block Erase, the Toggle Bit is valid after the last rising edge of the Block Erase $\overline{\text{WE}}$ pulse. The Toggle Bit is also active during the block erase time-out window.

In Byte Programming, if the block being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the block having changed. In Block Erase or Chip Erase, if all

selected blocks are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected blocks.

Toggling either $\overline{CE}$ or $\overline{OE}$ will cause DQ6 to toggle.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{DATA}$ Polling (DQ7), Toggle Bit (DQ6) and Erase Toggle Bit (DQ2) still function under this condition. The $\overline{CE}$ circuit will partially power down the device under those conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 3.

The DQ5 failure condition will also appear if the user tries to program a "1" to a location that was previously programmed to a "0". In this case, the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads valid data on DQ7 and DQ6 never stops toggling. Once the device exceeds the timing limits, DQ5 will indicate a "1". Please note that this is not a device failure condition since the device was used incorrectly. If timing limits are exceeded, reset the device. (See Table 6)

DQ3
Block Erase Timer

After the completion of the initial Block Erase command sequence, the Block Erase time-out window will begin. DQ3 will remain low until the time-out window is closed. $\overline{DATA}$ Polling and the Toggle Bit are valid after the initial Block Erase command sequence. (See Table 6)

If $\overline{DATA}$ Polling or the Toggle Bit indicates the device has been written with a valid Block Erase command, DQ3 may be used to determine if the block erase time-out window is still open. If DQ3 returns a "1", the internally controlled erase cycle has begun.

DQ2
Erase Toggle Bit

In the block erase operation, DQ2 will toggle with $\overline{OE}$ or $\overline{CE}$ when a read is attempted within the block that is being erased. DQ2 will not toggle if the read address is not within the block that is selected to be erased. In the chip erase operation, however, DQ2 will toggle with $\overline{OE}$ or $\overline{CE}$ regardless of the address given by the user. This is because all blocks are to be erased. (See Table 6)

Table 6. Status Register Bits

DQ	Name	Logic Level	Definition
7	$\overline{\text{DATA}}$ POLLING	'1'	Erase Complete or erase block in Erase suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erase block during Erase Suspend
		$\overline{\text{DQ7}}$	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	ERROR BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase suspend on currently addressed block. (When DQ5=1, Erase Error due to currently addressed block. Program during Erase Suspend on-going at current address
		DQ2	Erase Suspend read on non Erase Suspend Block

Notes:

DQ7 $\overline{\text{DATA}}$ Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E C operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

DQ5 Error Bit: set to "1' if failure in programming or erase

DQ3 P/E C Erase Time Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased block.

DATA PROTECTION

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the device will not accept commands on the rising edge of $\overline{WE}$.

Low V_{CC} Write Inhibit

During V_{CC} power-up or power-down, the EN20F002 locks out write cycles to protect against any unintentional writes. If $V_{CC} < V_{LOK}$, the command register is disabled and all internal program or erase circuits are disabled. Under this condition, the device will reset to the READ mode. Subsequent writes will be ignored until $V_{CC} > V_{LKO}$.

Write "Noise" Pulse Protection

Noise pulses less than 5ns on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will neither initiate a write cycle nor change the command register.

Logical Inhibit

If $\overline{OE} = V_{IL}$ or $\overline{CE}=V_{IH}$, or $\overline{WE}=V_{IH}$, writing is inhibited. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical "zero" and $\overline{OE}$ must be a logical "one".

Block Protection/Unprotection

When the device is shipped, all blocks are unprotected. Each block can be separately protected against data changes. Using hardware protection circuitry enabled at user's site with external programming equipment, both program and erase operations may be disabled for any specified block or combination of blocks.

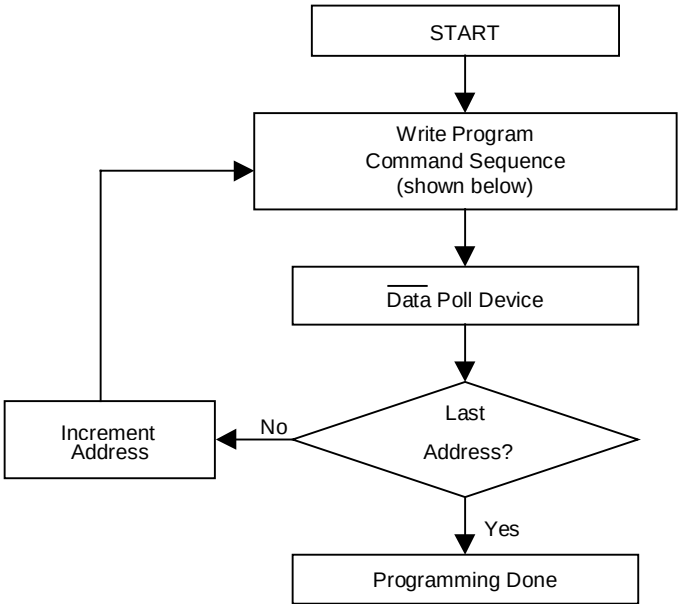
Verification of write protection for a specific block can be achieved with an Auto Select ID read command at location 02h where the address bits A17 - A13 select the defined block (see Table 5). A logical "1" at DQ0 means a protected block and a logical "0" means an unprotected block.

The Block Unprotect disables block protection in all blocks in one operation to implement code changes. A sector must be placed in protection mode using the protection algorithm mentioned above before unprotection can be executed.

Additional details on this feature are provided in a supplement, which can be obtained by contacting a representative of Eon Silicon Devices, Inc.

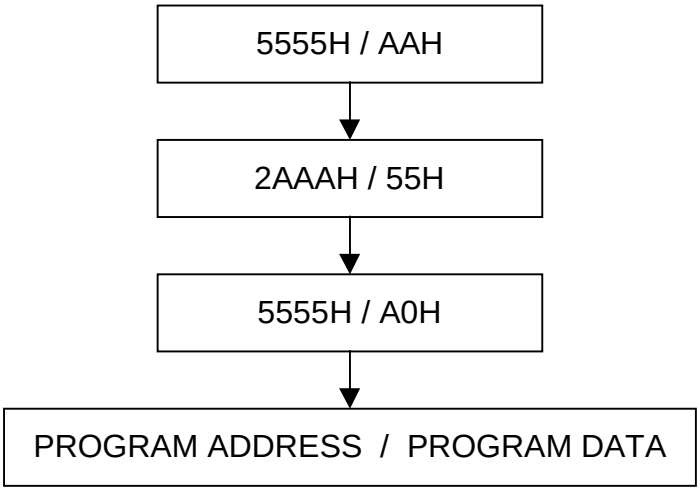
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

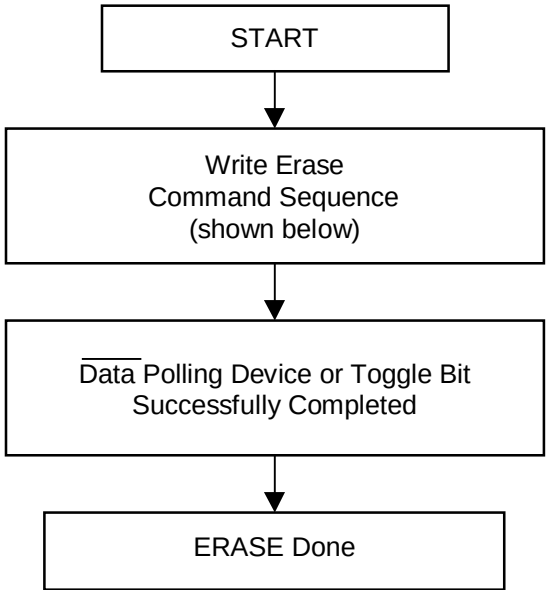


Flowchart 2. Embedded Program Command Sequence

See the Command Definitions section for more information.

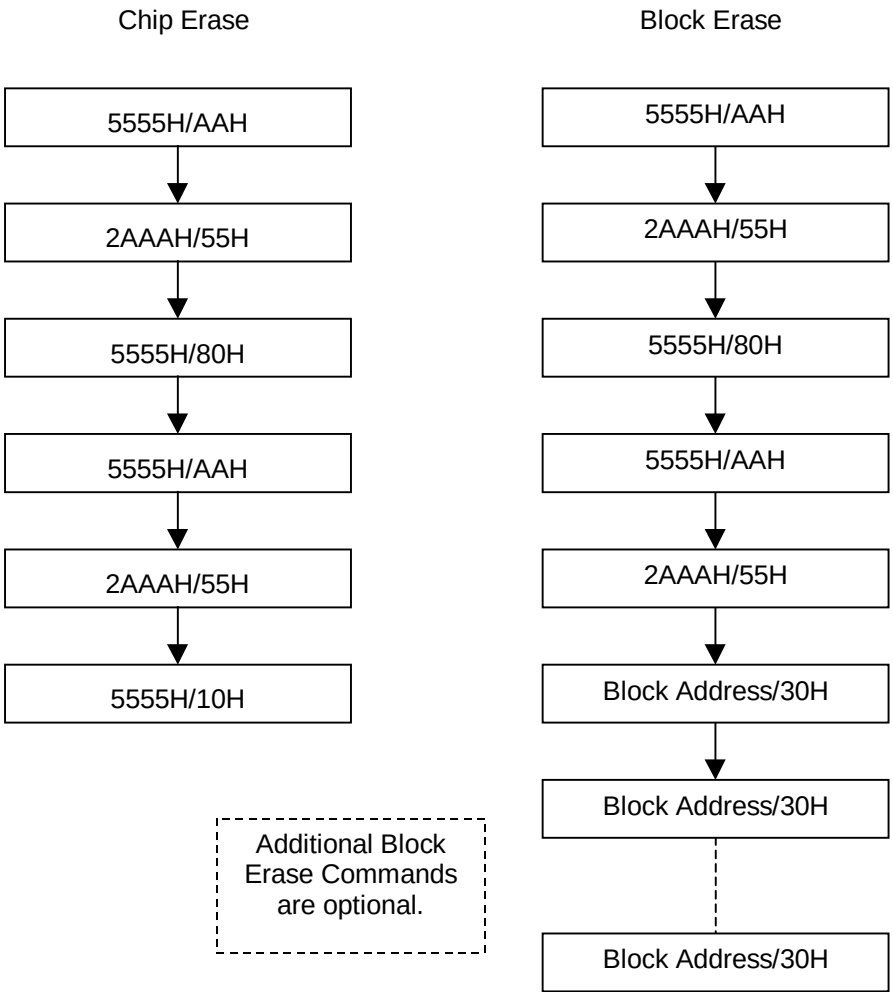


Flowchart 3. Embedded Erase

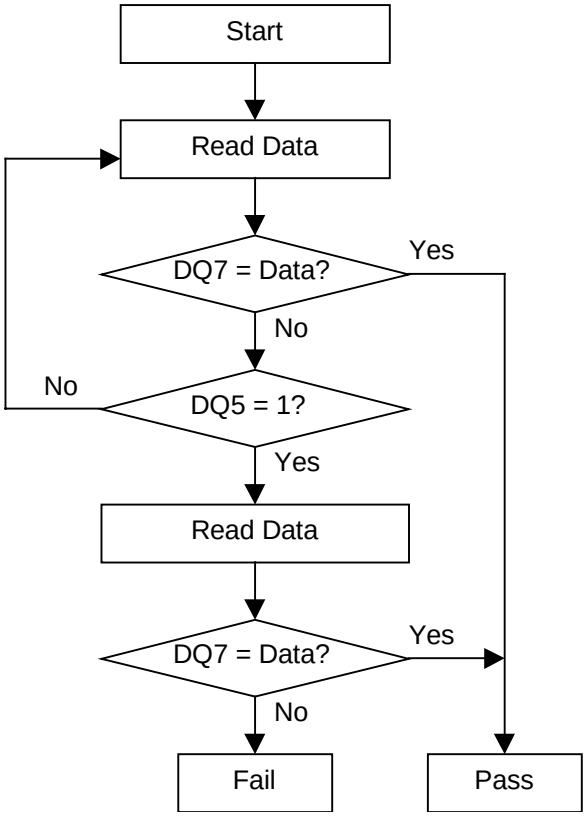


Flowchart 4. Embedded Erase Command Sequence

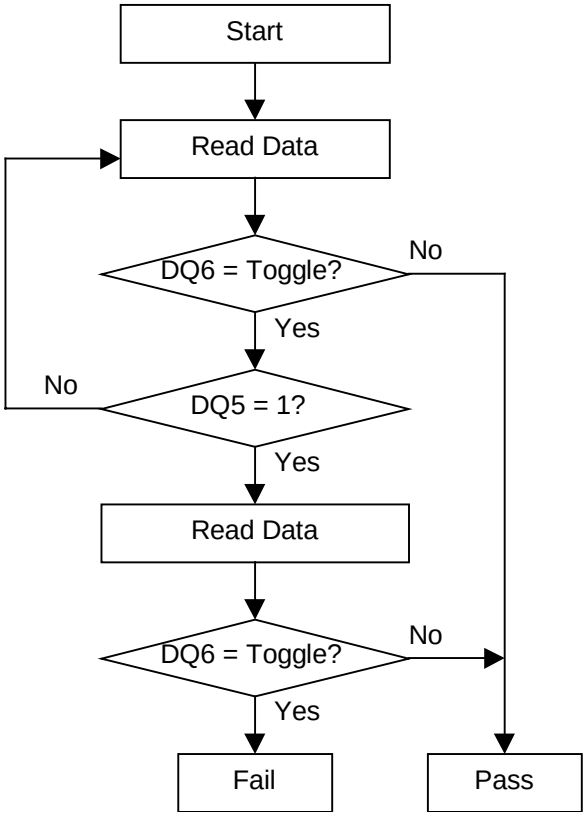
See the Command Definitions section for more information.



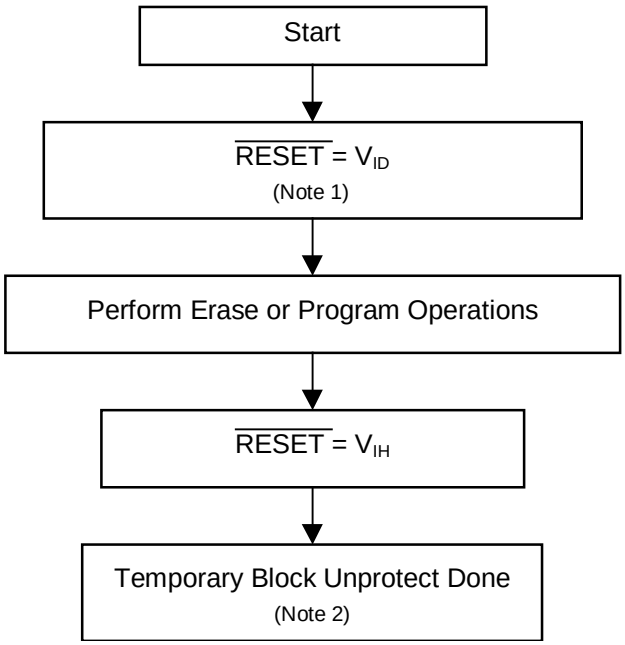
Flowchart 5. $\overline{\text{DATA}}$ Polling Algorithm



Flowchart 6. Toggle Bit Algorithm



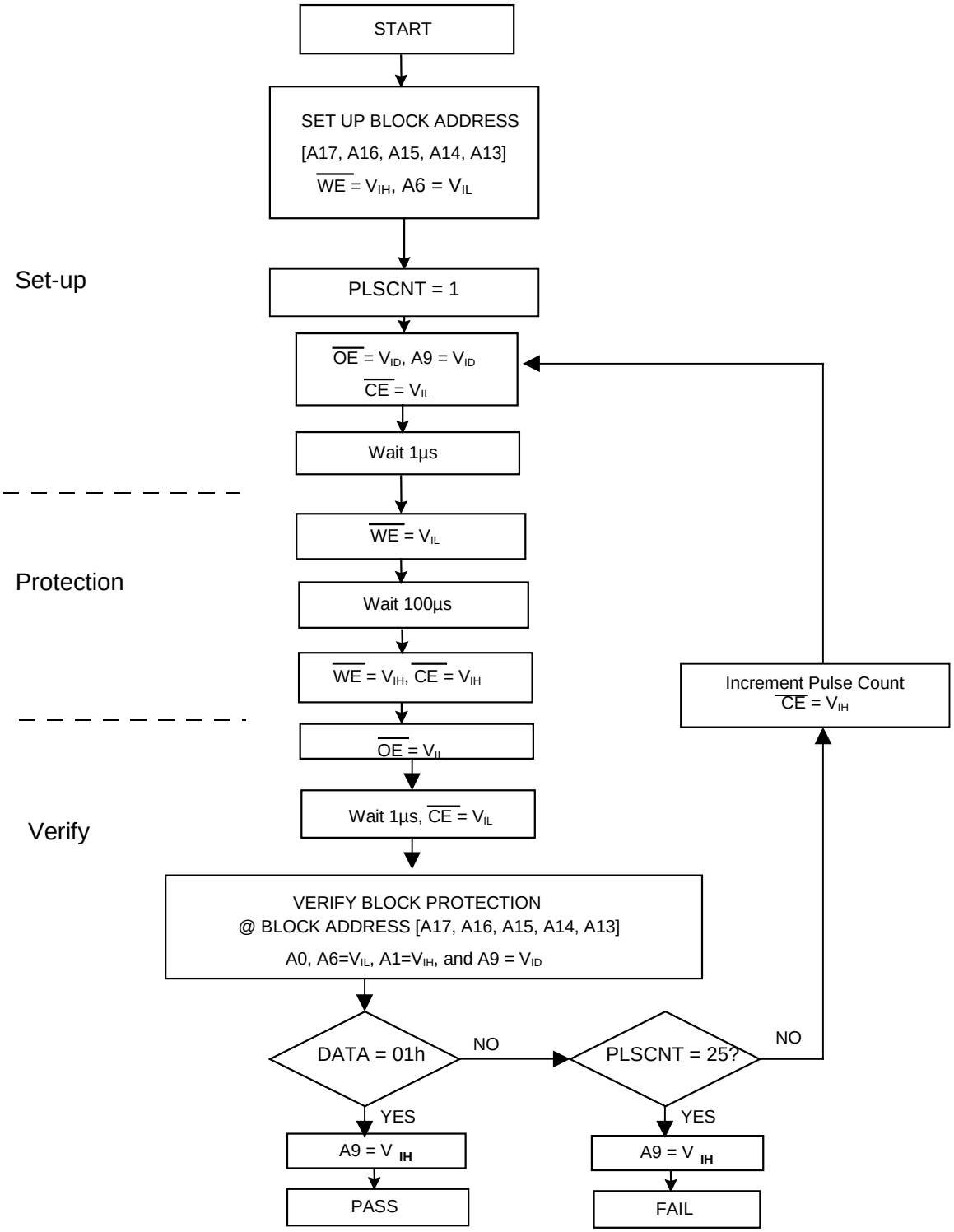
Flowchart 7. Temporary Block Unprotect Algorithm
(Not available for EN29F002N)



Notes:

1. All protected blocks unprotected.
2. All previous protected blocks are protected once again.

Flowchart 8. Block Protect Flowchart



Flowchart 9. Block Unprotect Flowchart

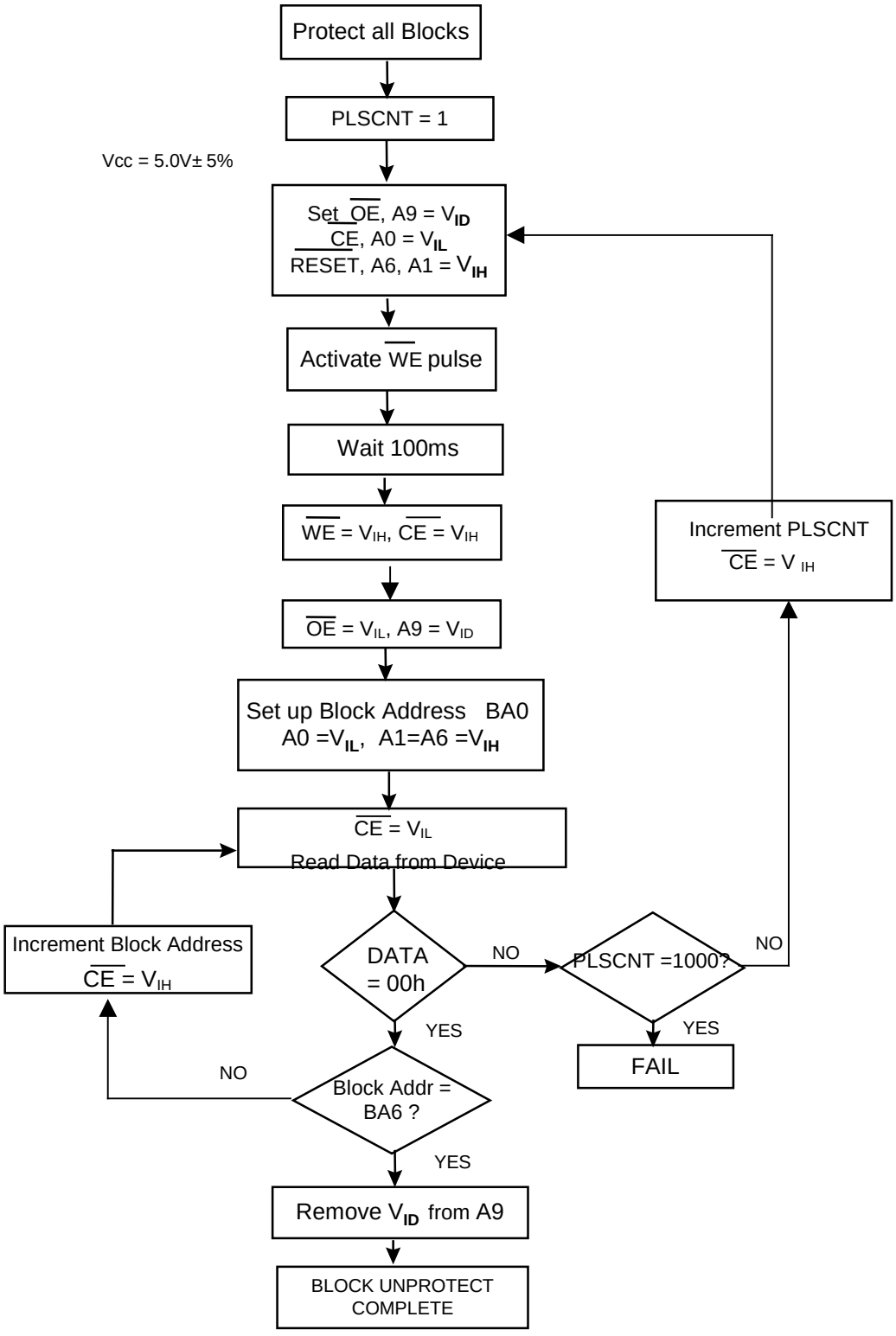


Table 7. DC Characteristics

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le Vcc$		±5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le Vcc$		±5	µA
I_{CC1}	Supply Current (read) TTL Byte	$E = V_{IL}$; $G = V_{IH}$; f = 6MHz		30	mA
I_{CC2}	Supply Current (Standby) TTL	$E = V_{IH}$		1.0	mA
I_{CC3}	Supply Current (Standby) CMOS	E = Vcc ± 0.2V		5.0	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Byte program, Block or Chip Erase in progress		30	mA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2	Vcc ± 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = -2.5 mA	2.4		V
	Output High Voltage CMOS	I_{OH} = -100 µA	Vcc - 0.4V		V
V_{ID}	A9 Voltage (Electronic Signature)		11.0	12.0	V
I_{ID}	A9 Current (Electronic Signature)	$A9 = V_{ID}$		100	µA
V_{LKO}	Supply voltage (Erase and Program lock-out)		3.2	4.2	V

Table 8. AC CHARACTERISTICS
Read-only Operations Characteristics

Parameter Symbols			Test Setup		Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		Min	45	55	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay	$\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z		Max	10	15	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z		Max	10	15	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first		Min	0	0	0	0	ns
	t_{Ready}	$\overline{RESET}$ Pin Low to Read Mode (n/a for EN29F002N)		Max	20	20	20	20	µs

Notes:

For -45,-55
Vcc = 5.0V ± 5%
Output Load : 1 TTL gate and 30pF
Input Rise and Fall Times: 5ns
Input Rise Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level, Input and Output: 1.5 V

For all others:
Vcc = 5.0V ± 10%
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level, Input and Output: 0.8 V and 2.0 V

Table 9. AC CHARACTERISTICS
Write (Erase/Program) Operations

Parameter Symbols					Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	MIn	0	0	0	0	ns
			Toggle and $\overline{DATA}$ Polling	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ SetupTime		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	35	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Block Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width (n/a for EN29F002N)		Min	500	500	500	500	ns
	t_{RSP}	$\overline{RESET}$ Setup Time (n/a for EN29F002N)		Min	4	4	4	4	µs

Table 10. AC CHARACTERISTICS
Write (Erase/Program) Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols					Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	0	0	0	0	0	ns
			Toggle and Data Polling	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ SetupTime		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	25	30	35	45	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Block Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width (n/a for EN29F002N)		Min	500	500	500	500	ns
	t_{RSP}	$\overline{RESET}$ Setup Time (n/a for EN29F002N)		Min	4	4	4	4	µs

Table 11. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Comments
	Typ	Max	Unit	
Block Erase Time	0.3	5	sec	Excludes 00H programming prior to erasure
Chip Erase Time	3	35	sec	
Byte Programming Time	7	200	µs	Excludes system level overhead
Chip Programming Time	2	5	sec	
Erase/Program Endurance	100K		cycles	Minimum 100K cycles guaranteed

Table 12. LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to Vss on all pins except I/O pins (including A9 and $\overline{OE}$, and $\overline{RESET}$)	-1.0 V	12.0 V
Input voltage with respect to Vss on all I/O Pins	-1.0 V	Vcc + 1.0 V
Vcc Current	200 mA	200 mA

Table 13. 32-PIN PLCC PIN CAPACITANCE @ 25°C, 1.0MHz

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	12	pF

Table 14. 32-PIN TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Table 15. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SWITCHING WAVEFORMS

Figure 5. AC Waveforms for READ Operations

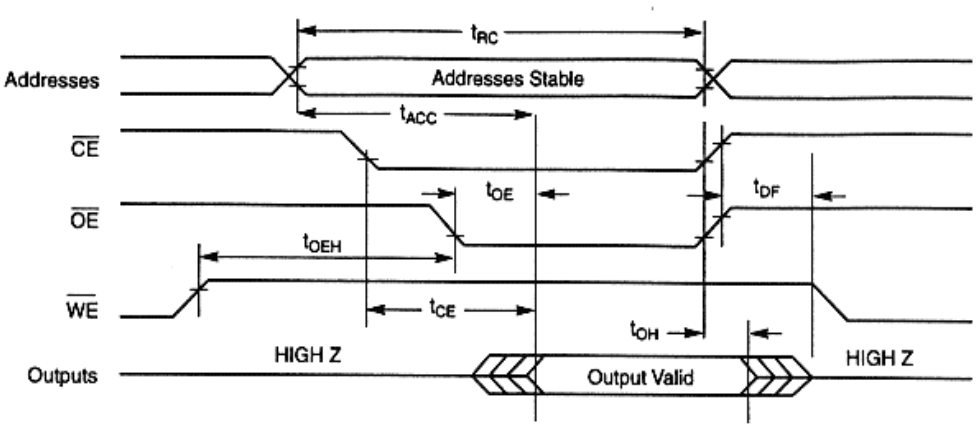
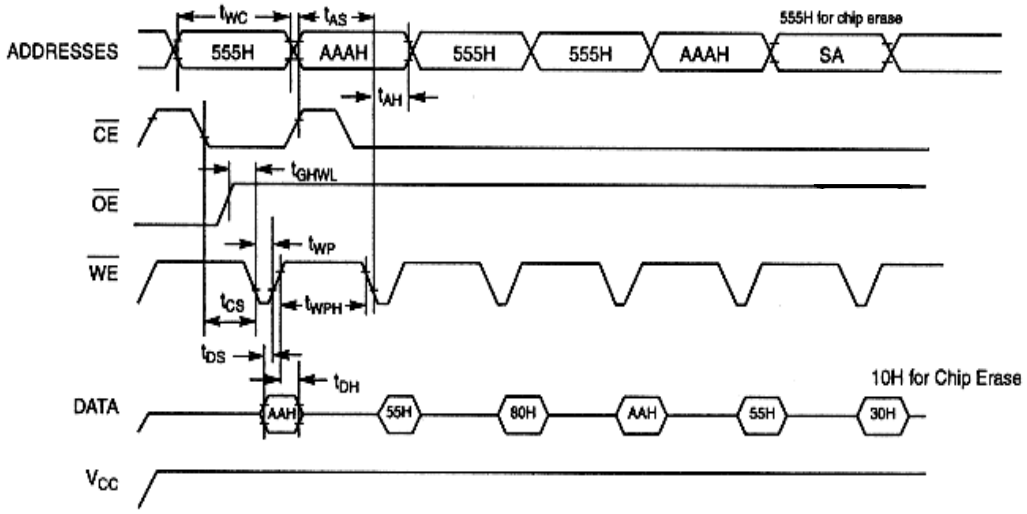


Figure 6. AC Waveforms for Chip/Block Erase Operations

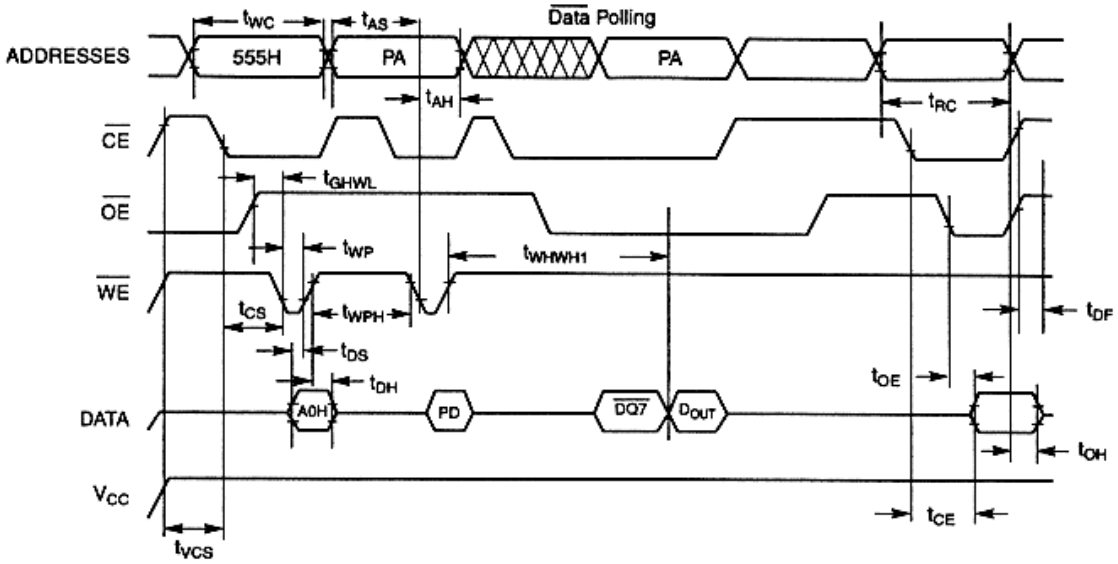


Notes:

1. SA is the block address for block erase.

SWITCHING WAVEFORMS (continued)

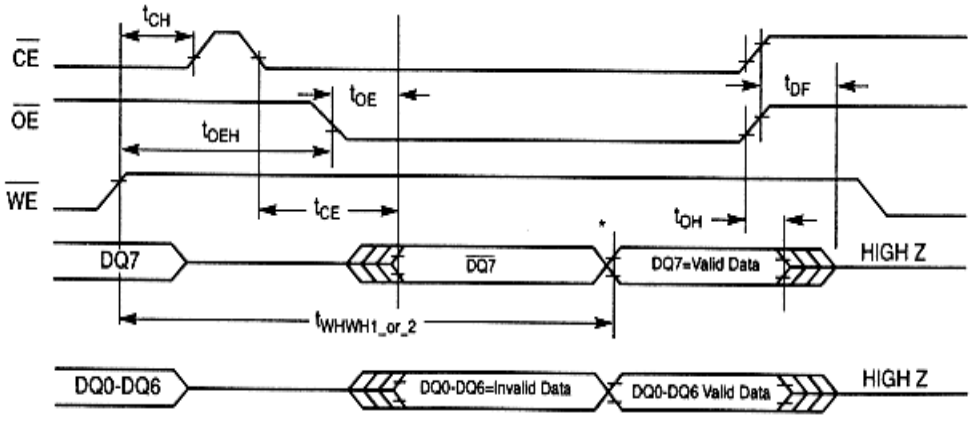
Figure 7. Program Operation Timings



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

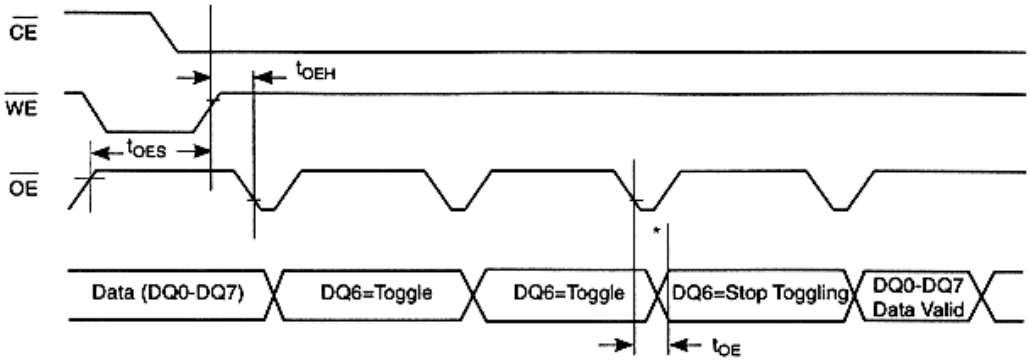
Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:

***DQ$_7$** = Valid Data (The device has completed the embedded operation).

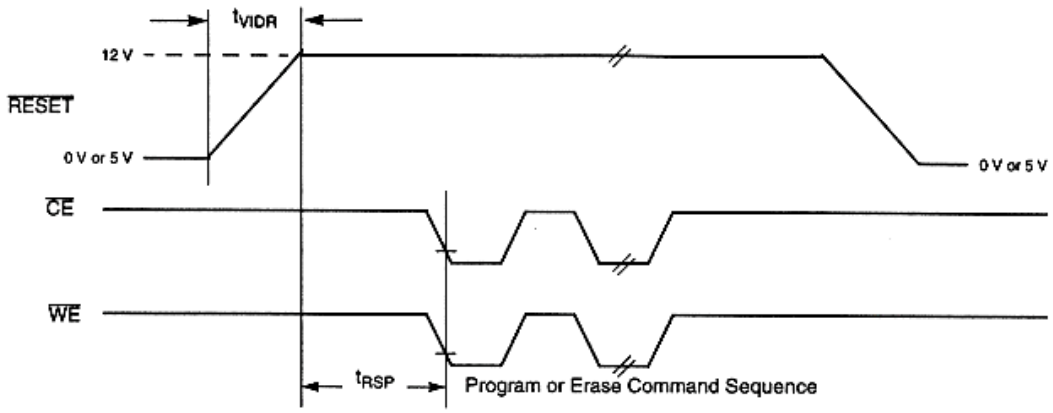
Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



Notes:

***DQ$_6$** stops toggling (The device has completed the embedded operation).

Figure 10. Temporary Block Unprotect Timing Diagram



SWITCHING WAVEFORMS (continued)

Figure 11. /RESET Timing Diagram

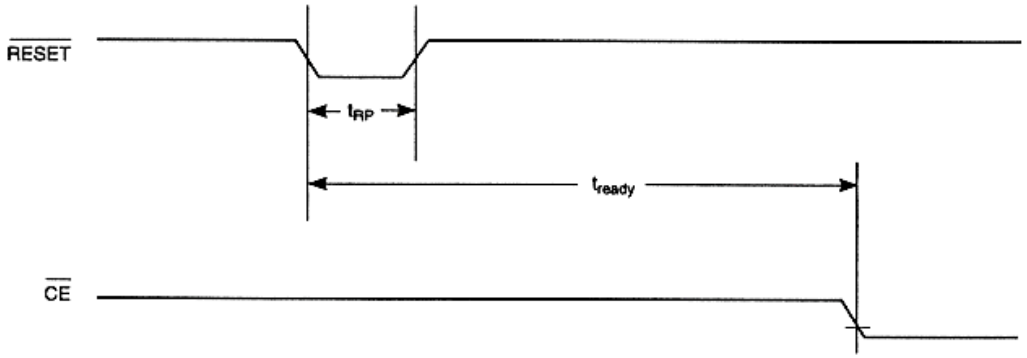
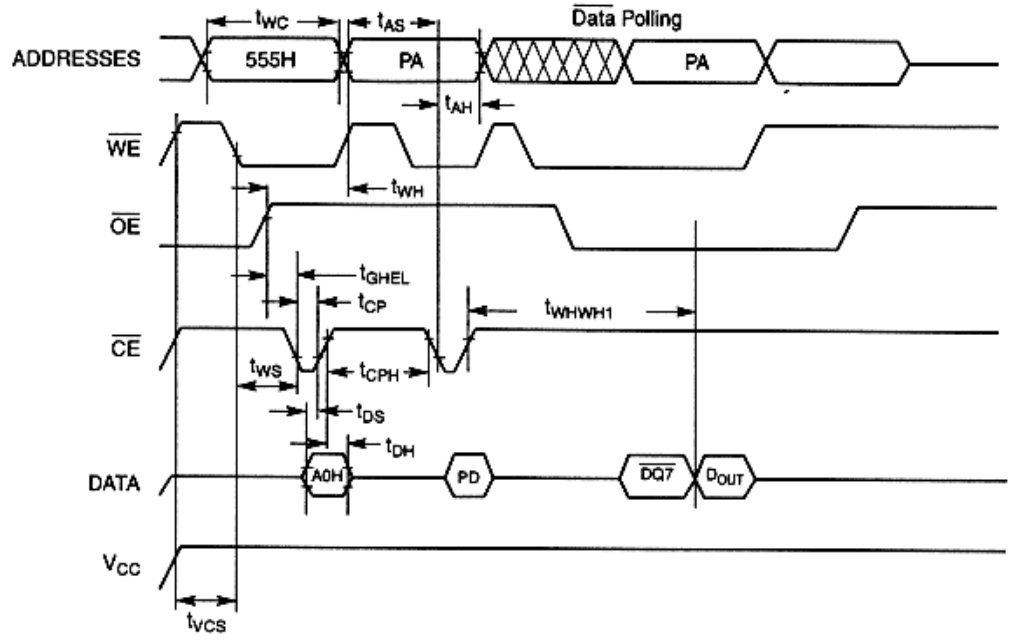


Figure 12. Alternate /CE Controlled Write Operation Timings

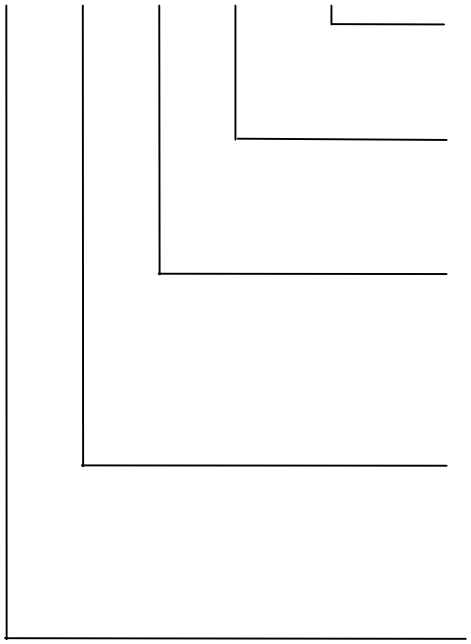


Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

ORDERING INFORMATION

EN29F002 T 45 P I



TEMPERATURE RANGE
(Blank) = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE
P = 32 Plastic DIP
J = 32 Plastic PLCC
T = 32 Plastic TSOP

SPEED
45 = 45ns
55 = 55ns
70 = 70ns
90 = 90ns

BOOT BLOCK ARCHITECTURE
T = Top Block
B = Bottom Block

BASE PART NUMBER
EN = EON Silicon Devices
29F = FLASH, 5V
002 = 256K x 8
(Blank) = with $\overline{\text{RESET}}$ function
N = without $\overline{\text{RESET}}$ function