

Features

32Kx32 bit CMOS Static
Random Access Memory

- Access Times 12, 15, 20, and 25ns
- Individual Byte Selects
- Output Enable Function
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Packaging

- 64 Pin SIMM, No. 54
- 64 Pin ZIP, No. 57
- JEDEC Standard Pinout
- Common Data Inputs and Outputs

Single +5V ($\pm 10\%$) Supply Operation

32Kx32 Static RAM

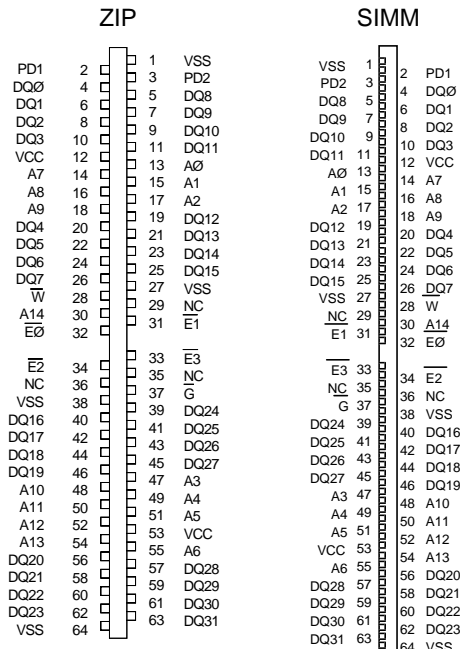
CMOS, High Speed Module

The ED18F3232C is a high speed megabit Static RAM module organized as 32Kx32. This module is constructed from four 32Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E0}$ - $\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The ED18F3232C is offered in both 64 lead SIMM and 64 pin ZIP packages, which enables one megabit of memory to be placed in less than 1.2 square inches of board space. All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

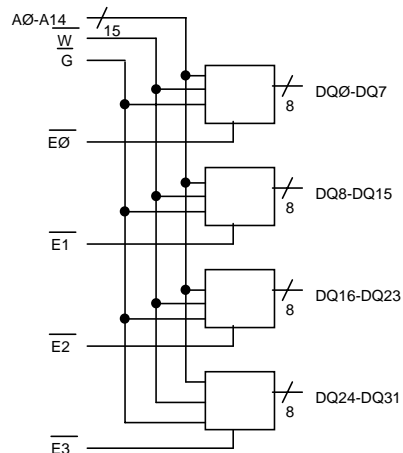
Pin Configurations and Block Diagram



PD1=Open
PD2 = VSS

Pin Names

A0-A14	Address Inputs
$\overline{E0}$ - $\overline{E3}$	Chip Enable
\overline{W}	Write Enable
\overline{G}	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	No Connection



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	4 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHOZ, TGHOZ and TWLOZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA,$	12ns	--	640	mA
Supply Current		Min Cycle	15ns	--	600	mA
			20ns	--	560	mA
			25ns	--	520	mA
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH, VIN \leq VIL$	--	--	225	mA
Supply Current		$VIN \geq VIH$				
Full Standby Power	ICC3	$\bar{E} \geq VCC-0.2V$	--	--	80	mA
Supply Current		$VIN \geq VCC-0.2V$ or				
CMOS		$VIN \leq 0.2V$				
Input Leakage Current	ILI	$VIN = 0V$ to VCC	--	--	±20	µA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	--	--	±20	µA
Output High Voltage	VOH	$IOH = -4.0mA$	2.4	--	--	V
Output Low Voltage	VOL	$IOL = 8.0mA$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{G}	\bar{E}	\bar{W}	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
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Address Lines	CI	60	pF
Data Lines	CD/O	20	pF
Chip Enable Line	CC	20	pF
Control Lines	CW	60	pF

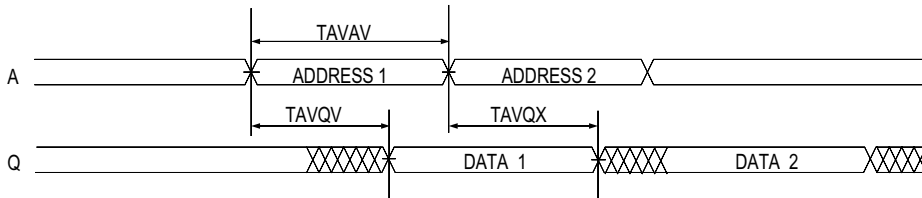
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

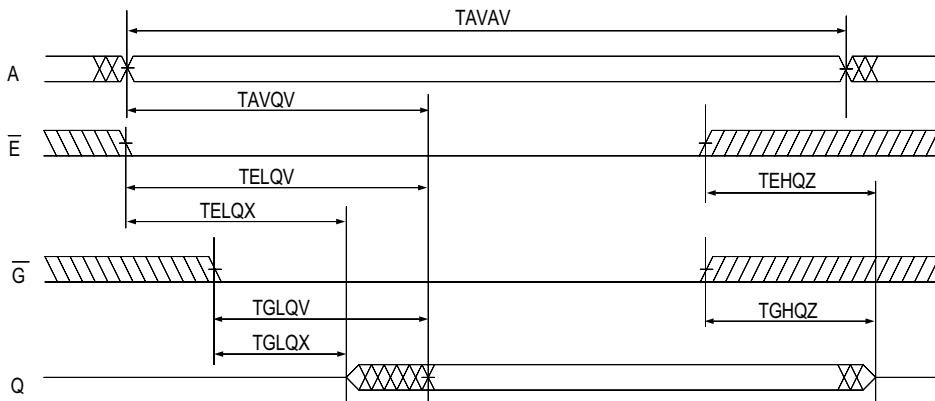
Parameter	Symbol		12ns		15ns		20ns		25ns	
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max Units
Read Cycle Time	TAVAV	TRC	12		15		20		25	ns
Address Access Time	TAVQV	TAA		12		15		20		25 ns
Chip Enable Access Time	TELOV	TACS		12		15		20		25 ns
Chip Enable to Output in Low Z (1)	TELOX	TCLZ	5		5		5		5	ns
Chip Disable to Output in High Z (1)	TEHOZ	TCHZ	0	5	0	9	0	11	0	13 ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3	ns
Output Enable to Output Valid	TGLQV	TOE		6		8		10		12 ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0	ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	5	0	8	0	10	0	10 ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - \bar{W} High, \bar{G} , \bar{E} Low



Read Cycle 2 - \bar{W} High

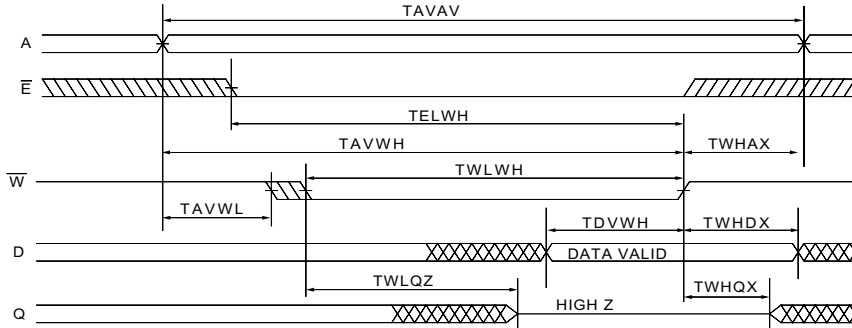


AC Characteristics Write Cycle

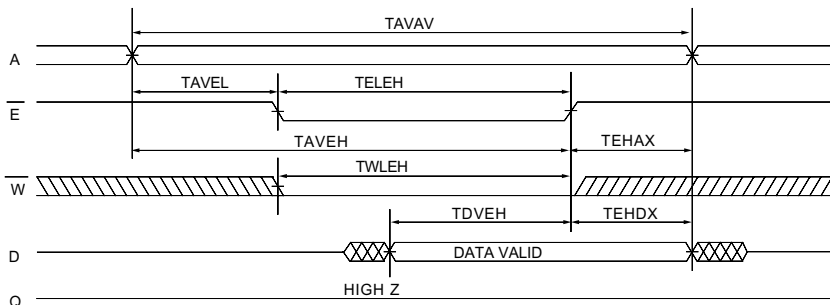
Parameter	Symbol		12ns		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	10		12		13		15		ns
	TELEH	TCW	10		12		13		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	10		12		13		15		ns
	TAVEH	TAW	10		12		13		15		ns
Write Pulse Width	TWLWH	TWP	10		11		12		15		ns
	TWLEH	TWP	10		11		12		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	3	0	3	0	3	0	5	ns
Data to Write Time	TDVWH	TDW	7		8		9		10		ns
	TDVEH	TDW	7		8		9		10		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - \bar{W} Controlled



Write Cycle 2 - \bar{E} Controlled



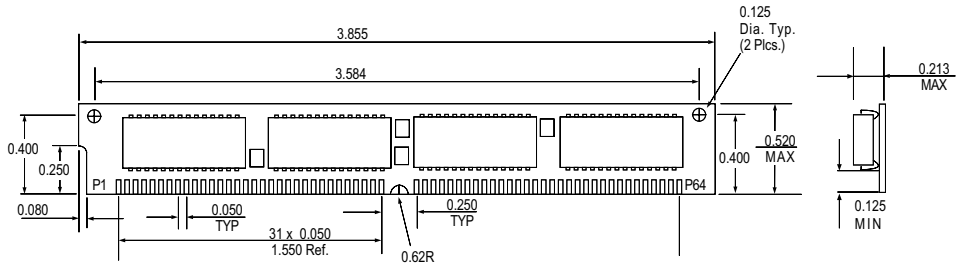
Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F3232C12MMC	12	54
EDI8F3232C15MMC	15	54
EDI8F3232C20MMC	20	54
EDI8F3232C25MMC	25	54
EDI8F3232C12MZC	12	57
EDI8F3232C15MZC	15	57
EDI8F3232C20MZC	20	57 </td
EDI8F3232C25MZC	25	57

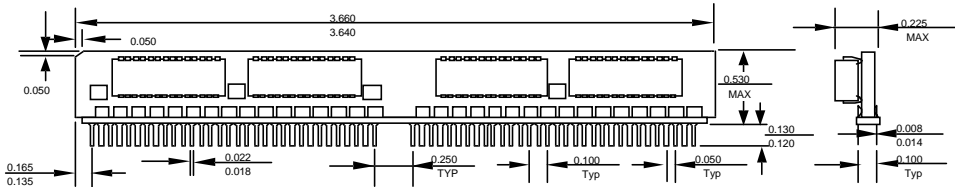
Note: To order an Industrial grade product change the last C in the suffix to I,
eg. EDI8F3232C25MZC becomes EDI8F3232C25MZI.

Package Description

Package No. 54
64 Pin SIMM Module



Package No. 57
64 Pin ZIP Module



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