AK5393

24-Bit, 96kHz Analog-to-Digital Converter

Features

- Proprietary dual-bit delta-sigma (ΔΣ) architecture
- Sampling rate from 1kHz to 108kHz
- Full differential inputs
- Dynamic range = 117dB
- Signal-to-noise = 117dB
- Signal-to-(Noise + Distortion) = 105dB
- On-chip linear phase digital anti-alias filter
  - Passband from 0 to 21.768kHz at fs = 48kHz
  - Ripple = 0.001dB
  - Stopband attenuation = 110dB
- Selectable digital HPF or offset calibration
- Power supplies
  - Analog: 5V ± 5%
  - Digital: from 3V to 5.25V
- Low power dissipation: 470mW
- Small 28-pin SOP package
- Pin compatible with the AK5391, AK5392, and AK5383

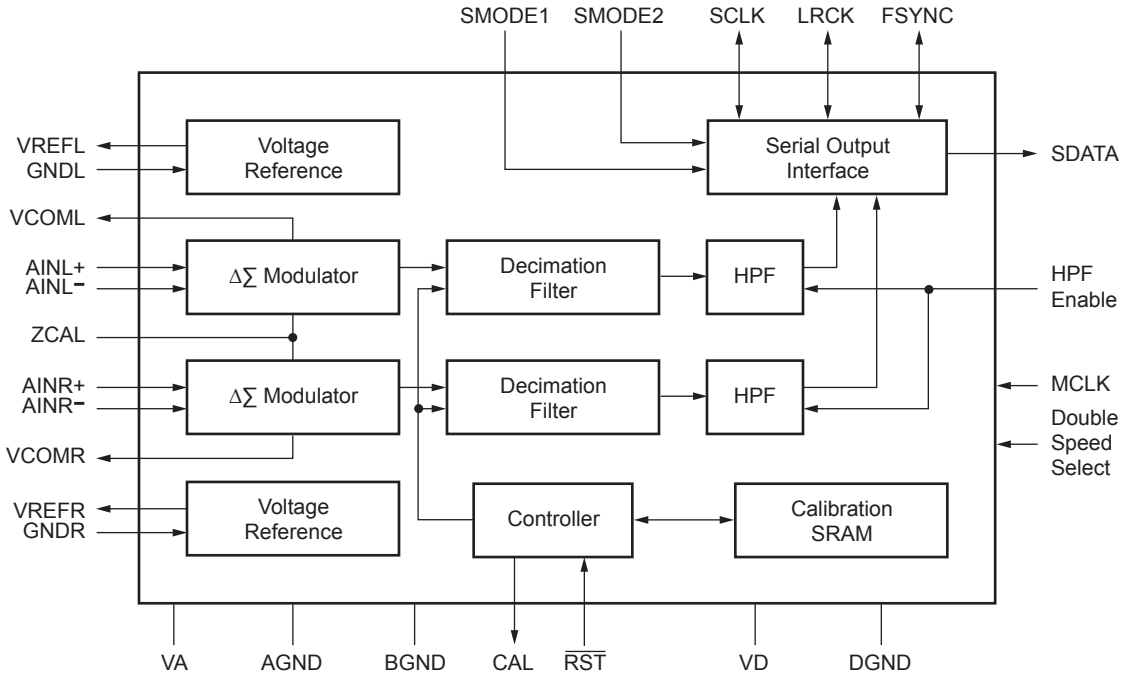
Description

The AK5393 is a 24-bit, 96kHz stereo Analog-to-Digital Converter (ADC) that offers up to 117dB of dynamic range and a 105dB Signal-to-(Noise + Distortion) Ratio. The improved dynamic range and lowered distortion are achieved using an innovative dual-bit ΣΔ architecture that reduces power consumption and improves reliability.

The AK5393 include full differential inputs for maximum signal range and performance. It also includes a reference filter and a digital decimation filter to minimize application requirements for anti-aliasing filtering. The user can select an internal HPF to eliminate DC inputs or offset calibration. The AK5393 outputs data at up to 108kHz, in several selectable formats.

The AK5393 is available in a space-saving 28-pin SOP package, and it operates over the full commercial temperature range: –10˚C to 70˚C.

Block Diagram



ASAHI KASEI MICROSYSTEMS CO., LTD.

Performance Specifications

Analog Characteristics

Ta = 25°C, VA = 5.0V, VD = 3.3V, AGND= SGND = DGND = 0V, fs = 48kHz, Signal Frequency = 1kHz, 24-bit output, and measurement frequency = 10Hz to 20kHz, unless otherwise specified.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Resolution				24	Bits
Analog Input Characteristics					
Dynamic Range	-60dBFS, A-Weighted	112	117		dB
Signal-to-Noise Ratio	A-Weighted	112	117		dB
Signal-to-(Noise + Distortion) Ratio	-1dBFS	98	105		dB
	-20dBFS		94		
	-60dBFS		54		
	-1dBFS, fs = 96kHz[1]	96	103		
	-20dBFS, fs = 96kHz[1]		85		
	-60dBFS, fs = 96kHz[1]		45		
Interchannel Isolation		110	120		dB
Interchannel Gain Mismatch			0.1	0.5	dB
Gain Drift				150	ppm/°C
Offset Error After Calibration	HPF = Off		±200	±1000	LSB[2]
	HPF = On		±1		
Offset Drift	HPF = Off		±10		LSB/°C
Offset Calibration Range	HPF = Off		±50		mV
Input Voltage	(AIN+) - (AIN-)	±2.3	±2.45	±2.6	V
Input Impedance		2.4	4		kΩ
Power Supplies					
Analog Power Supply Current			90	130	mA
Digital Power Supply Current			6	9	mA
	fs = 96kHz		9	14	
Power Dissipation			470	680	mW
Power Supply Rejection[3]			70		dB

Digital Characteristics

Ta = 25°C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Input					
High-Level Input Voltage		0.7VD			V
Low-Level Input Voltage				0.3VD	V
Input Leakage Current				±10	µA
Output					
High-Level Output Voltage	Iout = -20µA	VD - 0.1			V
Low-Level Output Voltage	Iout = 20µA			0.1	V

Performance Specification (Continued)

Filter Characteristics—fs = 48kHz

fs = 48kHz, Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = Low.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Filter (Decimation LPF)						
PB	Passband[4]		0		21.768	kHz
SB	Stopband[4]		26.232			kHz
PR	Passband Ripple				±0.001	dB
SA	Stopband Attenuation[5]		110			dB
GD	Group Delay[6]			38.7		1/fs
ΔGD	Group Delay Distortion			0		μs
ADC Digital Filter (HPF)						
FR	Frequency Response[4]	-3dB		1.0		Hz
		-0.1dB		6.5		

Filter Characteristics—fs = 96kHz

fs = 96kHz, Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, DFS = High.

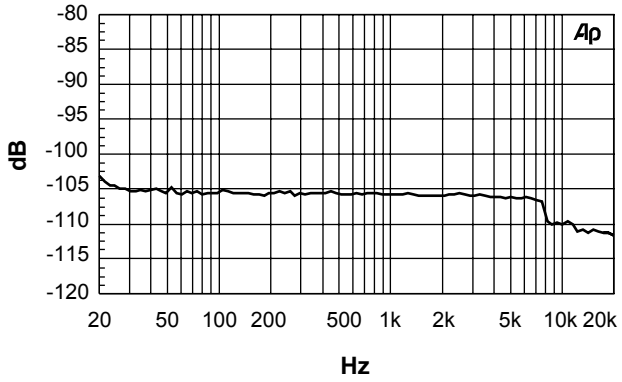
Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Filter (Decimation LPF)						
PB	Passband[4]		0		43.536	kHz
SB	Stopband[4]		52.464			kHz
PR	Passband Ripple				±0.003	dB
SA	Stopband Attenuation[7]		110			dB
GD	Group Delay[6]			38.8		1/fs
ΔGD	Group Delay Distortion			0		μs
ADC Digital Filter (HPF)						
FR	Frequency Response[4]	-3dB		2.0		Hz
		-0.1dB		13.0		

Notes:

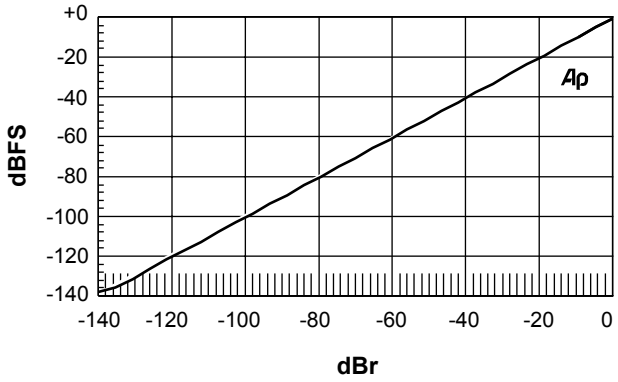
1. When fs = 96kHz, a measurement bandwidth of 40kHz is used.
2. The LSB refers to the Least Significant Bit of the 24-bit output data.
3. The Power Supply Rejection ratio is measured with a 1kHz, 20mV_{P-P} input to VA and VD. VREFH is held at a constant voltage.
4. The passband and stopband frequencies are proportional to fs.
5. The analog modulator samples the input at 6.144MHz for 48kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 21.768kHz, where n = 1, 2, 3, 4, ...
6. The Group Delay is the calculated delay time which takes place due to the digital filtering process. This time is taken from when the analog signal is input, to the time of setting the 24-bit data (from both channels) to the output register. When the HPF is on, this time is typically 40.7/fs if the DFS pin is Low, and 40.8/fs if the DFS pin is High.
7. The analog modulator samples the input at 6.144MHz for 96kHz output. There is no rejection of input signals which are multiples of the sampling frequency. That is, there is no rejection for signals of the following frequencies:
   n x 6.144MHz ± 43.536kHz, where n = 1, 2, 3, 4, ...

Typical Performance Curves

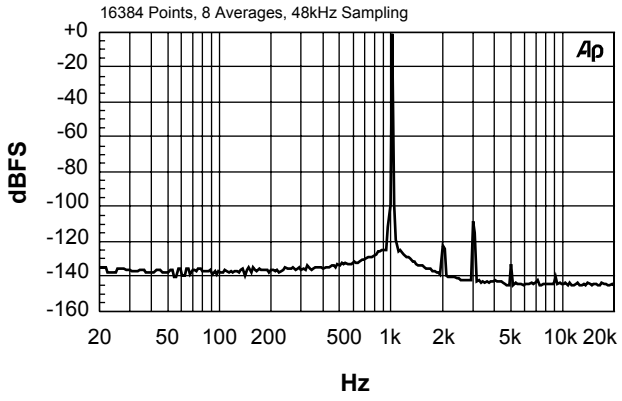
THD + N vs. Frequency



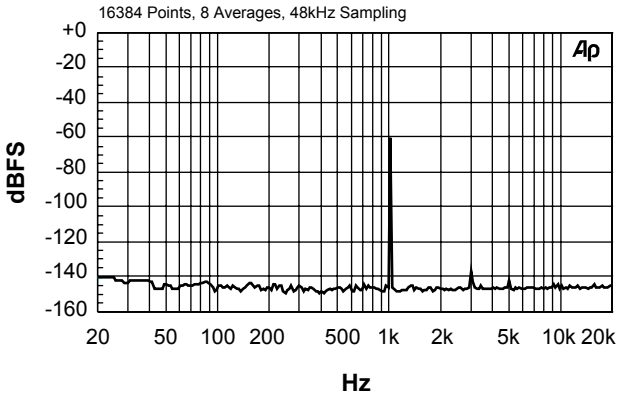
Linearity



0dB FFT



-60dB FFT



Absolute Maximum Ratings

AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

Parameter		Min.	Max.	Units
Power Supplies				
VA	Analog Power Supply	-0.3	6.0	V
VD	Digital Power Supply	-0.3	6.0	V
ΔGND[1]	|SGND - DGND|		0.3	V
IIN	Input Current—All pins except supply pins		±10	mA
VINA	Analog Input Voltage	-0.3	VA + 0.3	V
VIND	Digital Input Voltage	-0.3	VD + 0.3	V
Temperature				
Ta	Ambient Operating Temperature (Power Applied)	-10	70	°C
Tstg	Storage Temperature	-65	150	°C

Note:

1. AGND and SGND must be at the same voltage.

Caution:
Exceeding minimum and maximum ratings may result in damage to the device.

Recommended Operating Conditions

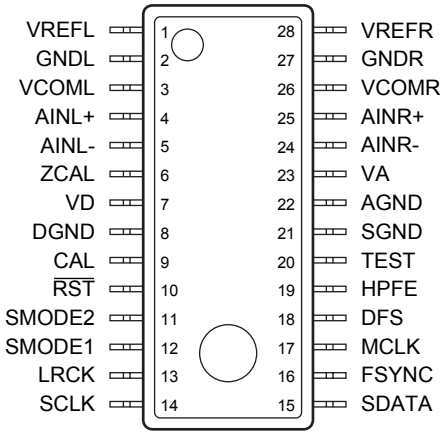
AGND, SGND, and DGND = 0V. All voltages are with respect to ground.

Parameter		Min.	Typ.	Max.	Units
Power Supplies[1]					
VA	Analog Power Supply	4.75	5.0	5.25	V
VD	Digital Power Supply	3.0	3.3	5.25	V

Note:

1. The VA and VD power-up sequences are not critical.

Pin Descriptions



Note:
See Table 1 for compatibility with other AKM devices.

Pin Descriptions

No.	Pin Name	I/O	Pin Function and Description
1	VREFL	O	**Left Channel Reference Voltage.** VREFL = 3.75V. This pin is normally connected to the GNDL pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information.
2	GNDL	-	**Left Channel Reference Ground.** GNDL = 0V.
3	VCOML	O	**Left Common Voltage.** VCOML = 2.75V.
4	AINL+	I	**Left Channel Analog Positive Input.**
5	AINL-	I	**Left Channel Analog Negative Input.**
6	ZCAL	I	**Zero Calibration Control.** This pin controls the calibration reference signal. When ZCAL is Low, the VCOML and VCOMR are selected. When High, the analog inputs (AINL+, AINL-, AINR+, and AINR-) are used for the reference level.
7	VD	-	**Digital Power Supply.** VD = 3.3V.
8	DGND	-	**Digital Ground.** DGND = 0V.
9	CAL	O	**Calibration Active Signal.** When this pin outputs a High signal, it shows that the offset calibration cycle is in progress. The offset calibration cycle starts when the RST pin goes High. The CAL pin goes Low after 8704 clock cycles when DFS is Low or after 17408 cycles when DFS is High.
10	$\overline{\text{RST}}$	I	**Reset.** When this pin is Low, the digital section is powered down. When this pin returns to High, an offset calibration cycle starts. An offset calibration cycle should always be initiated upon powering up the device.
11	SMODE2	I	**Serial Interface Mode Select.** The serial interface mode data should always be MSB first, 2's complement formatted. See Table 3 for these pin definitions.
12	SMODE1	I	
13	LRCK	I/O	**Left Channel and Right Channel Select Clock.** During reset—when the SMODE1 pin is High—the LRCK pin goes High when the SMODE2 pin is Low, and the LRCK pin goes Low when the SMODE2 pin is High.
14	SCLK	I/O	**Serial Data Clock.** Data is clocked on the falling edge of SCLK. In the slave mode, the SCLK pin requires a clock greater than 48fs. In the master mode, this pin outputs a 128fs (when DFS is Low) clock or a 64fs clock. SCLK is Low during reset.
15	SDATA	O	**Serial Data Output.** Serial data output is MSB first and 2's complement formatted. This pin is low during reset.
16	FSYNC	I/O	**Frame Synchronization Signal.** In slave mode, when FSYNC is High, the data bits are clocked on SDATA. In the master mode, FSYNC outputs a 2fs clock and it is Low during reset.

Pin Descriptions (Continued)

No.	Pin Name	I/O	Pin Function and Description
17	MCLK	I	**Master Clock Input.** Set the DFS pin Low for a 256fs input clock. Set the DFS pin High for a 128fs clock.
18	DFS	I	**Double Speed Sampling Mode.** When this pin is Low, the chip is in normal speed mode. When High, the double speed mode is selected.
19	HPFE	I	**High Pass Filter Enable.** When this pin is High, the high pass filter is enabled. When Low, this pin is disabled.
20	TEST	I	**Test.** This pin should be connected to ground.
21	SGND	-	**Substrate Ground.** SGND = 0V.
22	AGND	-	**Analog Ground.** AGND = 0V.
23	VA	-	**Analog Power Supply.** VA = 5V.
24	AINR-	I	**Right Channel Analog Negative Input.**
25	AINR+	I	**Right Channel Analog Positive Input.**
26	VCOMR	O	**Right Common Voltage Pin.** VCOMR = 2.75V.
27	GNDR	-	**Right Channel Reference Ground**. GNDR = 0V.
28	VREFR	O	**Right Channel Reference Voltage.** VREFR = 3.75V. This pin is normally connected to the GNDR pin through a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor in parallel. Refer to the Design Considerations section for additional information.

Note:

1. All input pins, except pull-down pins, should not be left floating.

Table 1. AK5393 Compatibility with the AK5392

	AK5393	AK5392	AK5391	AK5383
Pin 2	GNDL	GNDL	VREFL-	GNDL
Pin 18	DFS	CMODE	CMODE	DFS
Pin 19	HPFE	HPFE	SEL24	HPFE
Pin 27	GNDR	GNDR	VREFR-	GNDR
Maximum fs	108kHz	54kHz	54kHz	108kHz
Master Clock at 48kHz	256fs	256fs or 384fs	256fs or 384fs	256fs
Master Clock at 96kHz	128fs	N/A	N/A	128fs

Swithching Characteristics

Ta = 25˚C, VA = 5.0V ± 5%, VD = 3.0V to 5.25V, C_L = 20pF.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
Control Clock Frequency						
fCLK	Master Clock Frequency	256fs	0.256	12.288	13.824	MHz
tCLKL	Clock Pulse Width Low		29			ns
tCLKH	Clock Pulse Width High		29			ns
fSLK	Serial Data Output Clock (SCLK) Frequency			6.144	6.912	MHz
fs	Channel Select Clock (LRCK) Frequency		1	48	108	kHz
Duty Cycle			25		75	%
Serial Interface Timing—Slave Mode[1] (SMODE = Low)						
tSLK	SCLK Period		144.7			ns
tSLKL	SCLK Pulse Width Low		65			ns
tSLKH	SCLK Pulse Width High		65			ns
tSLR	SCLK Falling Edge to LRCK Edge	Note 2	-45		45	ns
tDLR	LRCK Edge to SDATA MSB Valid				45	ns
tDSS	SCLK Falling Edge to SDATA Valid				45	ns
tSF	SCLK Falling Edge to FSYNC Edge		-45		45	ns
Serial Interface Timing—Master Mode (SMODE = High)						
tSCLK	SCLK Frequency	DFS = Low		128fs		Hz
		DFS = High		64fs		
SCLK Frequency Duty Cycle				50		%
fFSYNC	FSYNC Frequency			2fs		Hz
FSYNC Frequency Duty Cycle				50		%
tSLR	SCLK Falling Edge to LRCK Edge		-20		20	ns
tLRF	LRCK Edge to FSYNC Rising Edge			1		tSLK
tDSS	SCLK Falling Edge to SDATA Valid				45	ns
tSF	SCLK Falling Edge to FSYNC Edge		-20		20	ns
Reset and Calibration Timing						
tRTW	$\overline{\text{RST}}$ Pulse Width		150			ns
tRCR	$\overline{\text{RST}}$ Falling to CAL Rising Edge				50	ns
tRCF	$\overline{\text{RST}}$ Rising to CAL Falling Edge	Note 3		8704		1/fs
tRTV	$\overline{\text{RST}}$ Rising Edge to SDATA Valid	Note 3		8960		1/fs

Notes:

1. Refer to the Serial Data Interface section.
2. The specified LRCK edges do not coincide with the rising edges of SCLK.
3. tRCF and tRTV specify the number of LRCK rising edges after $\overline{\text{RST}}$ is brought High. This value is given for when the device is operated in master mode. In slave mode, this value is one LRCK clock (1/fs) longer. When the DFS is High, the number of cycles, 1/fs, is doubled.

Timing Diagrams

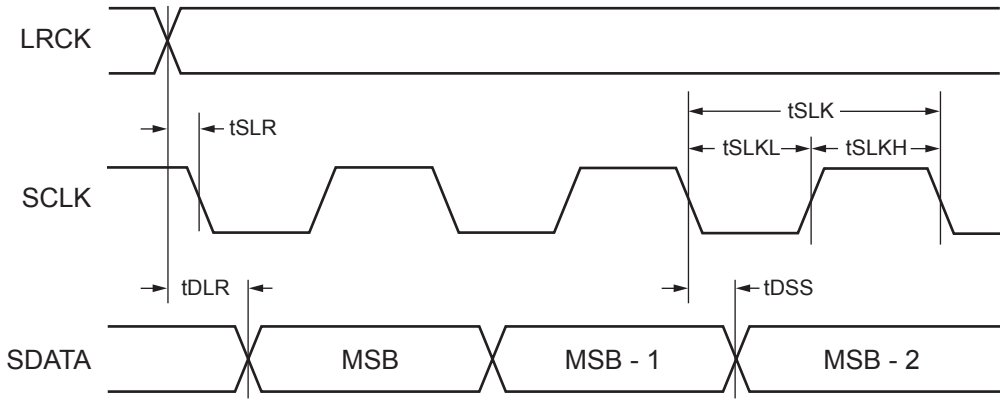


Figure 1. Serial Data Timing (Slave Mode, FSYNC = High)

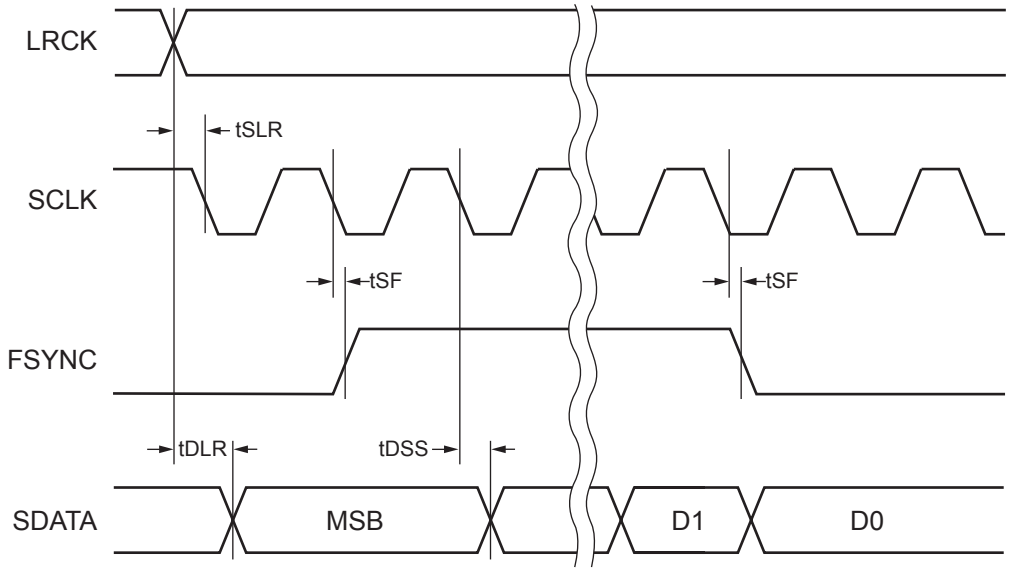


Figure 2. Serial Data Timing (Slave Mode)

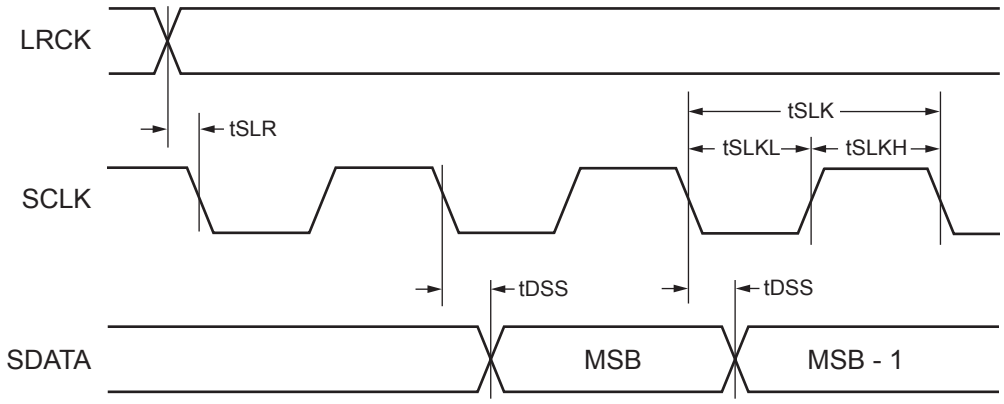


Figure 3. Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)

Timing Diagrams (Continued)

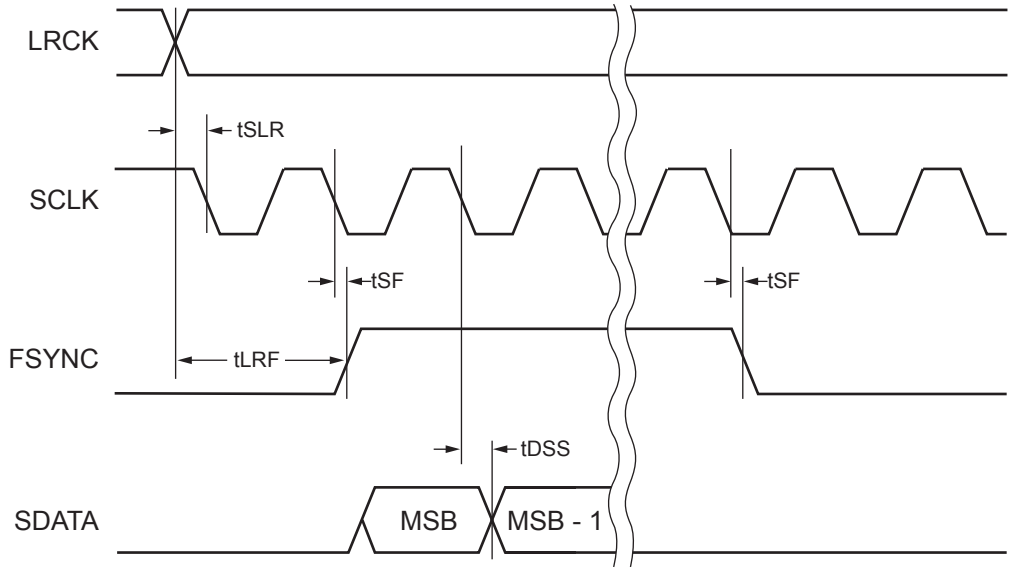


Figure 4. Serial Data Timing (Master Mode and I^2S Master Mode, DFS = Low)

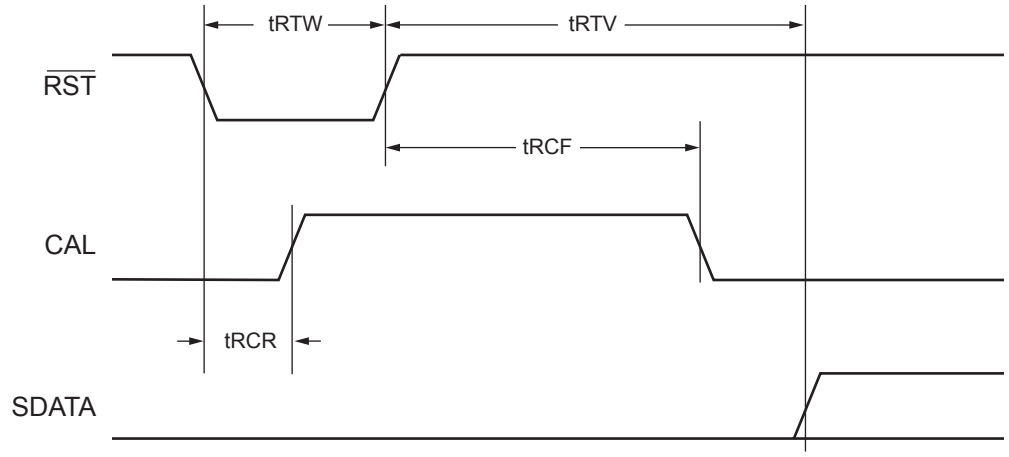


Figure 5. Reset and Calibration Timing

Device Operation

System Clock Input

Three clocks are required to operate the AK5393: the Master Clock (MCLK), the Left/Right Channels Select Clock (LRCK), and the Serial Data Clock (SCLK). Refer to Table 1. The MCLK should be synchronized with the LRCK, but the phase is not critical. MCLK should be 256fs when in the normal sampling mode (i.e. DFS = Low), and should be 128fs when in the double sampling mode. Table 2 shows the standard audio word rates and their corresponding frequencies.

Table 1. System Clocks

	Normal Speed (DFS = Low)	Double Speed (DFS = High)
LRCK (maximum)	54kHz	108kHz
BICK	Up to 128fs	Up to 64fs
MCLK	256fs	128fs

Table 2. System Clocks

fs	MCLK	SCLK
32.0kHz	8.1920MHz	4.0960MHz
44.1kHz	11.2896MHz	5.6448MHz
48.0kHz	12.2880MHz	6.1440MHz
96.0kHz	12.2880MHz	6.1440MHz

The AK5393 includes a phase detect circuit for the LRCK; thus, by changing the clock frequencies, the device is reset automatically when synchronization of MCLK on LRCK is not maintained. With this feature, resetting the AK5393 is only needed during power-up.

Ideally, all external clocks—MCLK, BICK, and LRCK—should always be present whenever the AK5393 is in normal operation (that is, when $\overline{RST}$ is High). In real applications, however, one or more of these clocks may not be present for a short amount of time. When this occurs, the AK5393 should be reset by setting the $\overline{RST}$ pin Low, which resets and powers down the device. Once all the clocks have been reinstated, the $\overline{RST}$ pin can again be set High for normal operation, completing the reset procedure.

Caution:
Due to its internal dynamic refresh logic, prolonged periods of time without external clock input may result in damage to the device.

Serial Data Interface

The AK5393 supports four serial data formats which can be selected using the SMODE1 and SMODE2 pins. Refer to Table 3. The data format is MSB first and 2's complement. Figures 6 through 9 show the timing diagrams for the four different types of serial data formats.

Table 3. Serial Interface Formats

Timing Diagram	SMODE2	SMODE1	Mode	LRCK	
				Left Channel	Right Channel
Figure 6	L	L	Slave Mode	H	L
Figure 7	L	H	Master Mode	H	L
Figure 8	H	L	I^2S Slave Mode	L	H
Figure 9	H	H	I^2S Master Mode	L	H

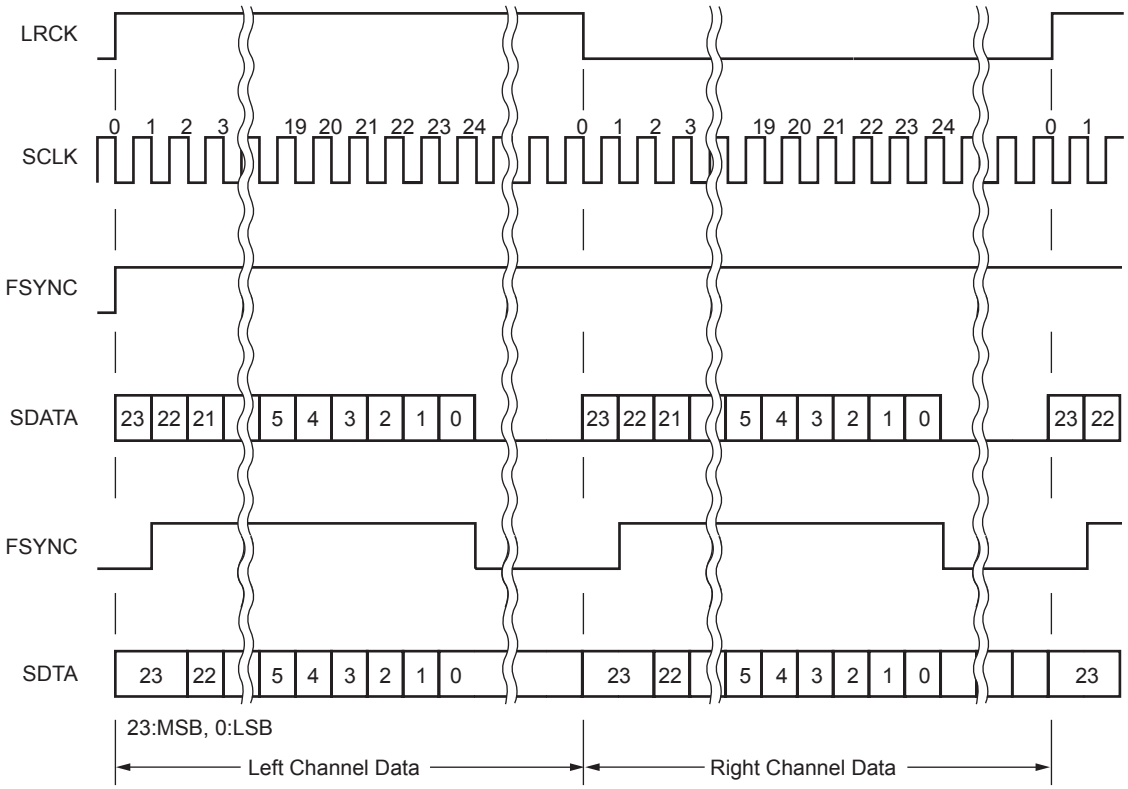


Figure 6. Serial Data Timing—Slave Mode

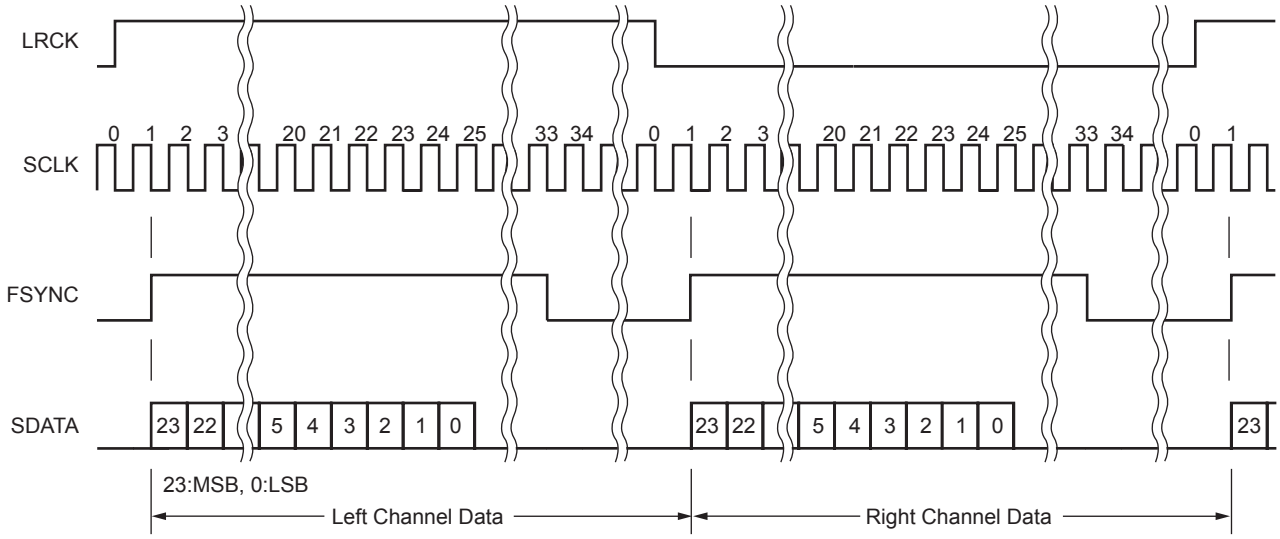


Figure 7. Serial Data Timing—Master Mode (DFS = Low)

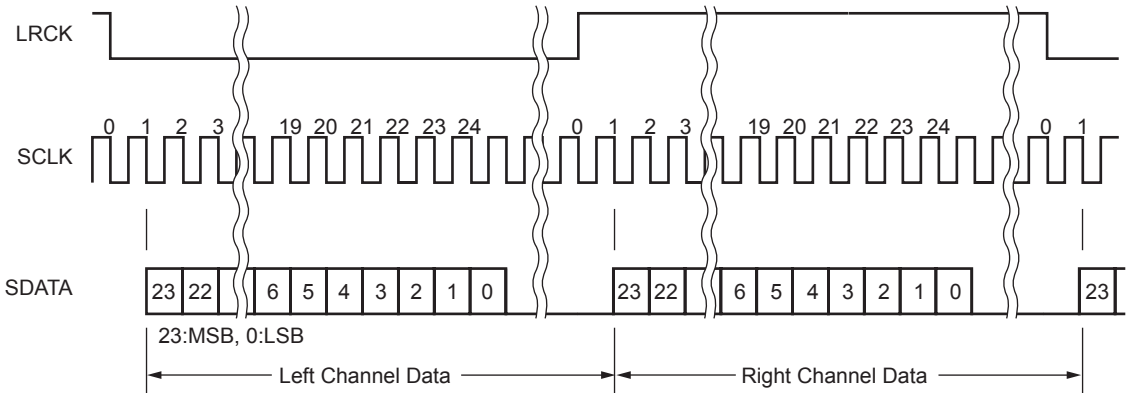


Figure 8. Serial Data Timing—I²S Slave Mode

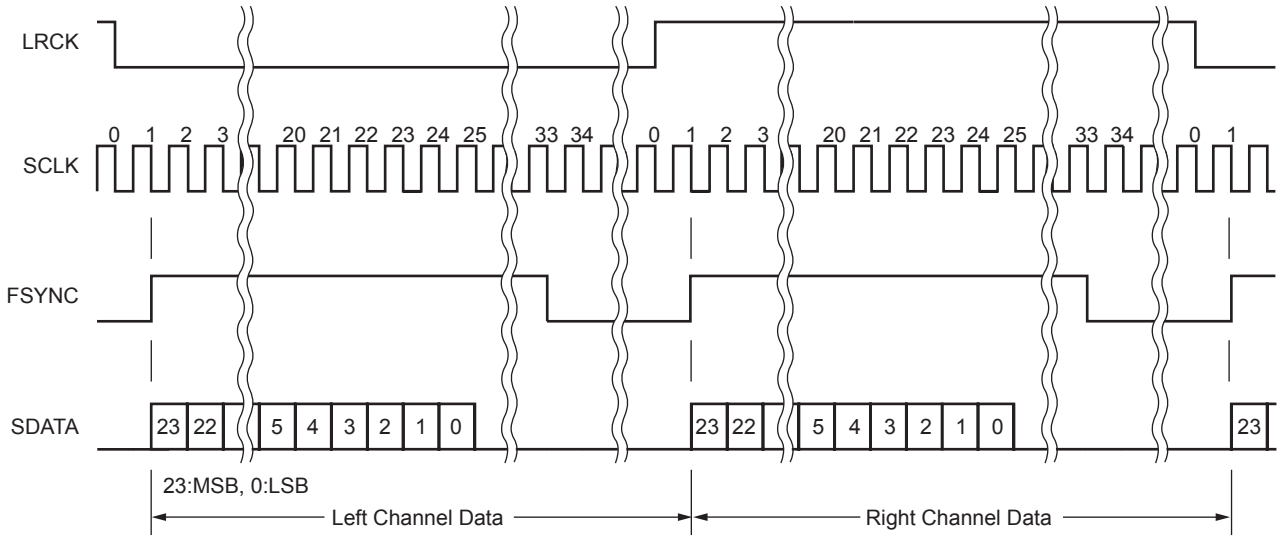


Figure 9. Serial Data Timing—I²S Master Mode (DFS = Low)

Offset Calibration

When the $\overline{\text{RST}}$ pin goes Low, the digital section of the AK5393 is powered down. When this pin returns to High, an offset calibration cycle is started. Such cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the AK5393 measures and store the calibration values of each channel into the registers. These calibration values are subtracted from all future outputs. Calibration values may be obtained from the analog input pins (AINL-, AINL+, AINR-, and AINR+) or from the common voltage pins (VCOML and VCOMR) depending on the state of the ZCAL pin. When ZCAL is High, voltages from the analog input pins are measured. When ZCAL is Low, the common voltage pins are measured. The CAL pin is High during calibration.

Digital High Pass Filter

The AK5393 includes a digital High Pass Filter (HPF) used for DC offset cancellation. The cut-off frequency, fc, for the HPF is 1Hz at fs = 48kHz. This frequency also scales with the sampling rate, fs. The cut-off frequency can be calculated by fc = fs/48k.

Design Considerations

Figure 10 shows a system connection diagram. An evaluation board for this device is available, the AKD5393 (see the Ordering Information section). This board demonstrates the applications circuits, an optimum layout, power supply arrangements, and measurement results.

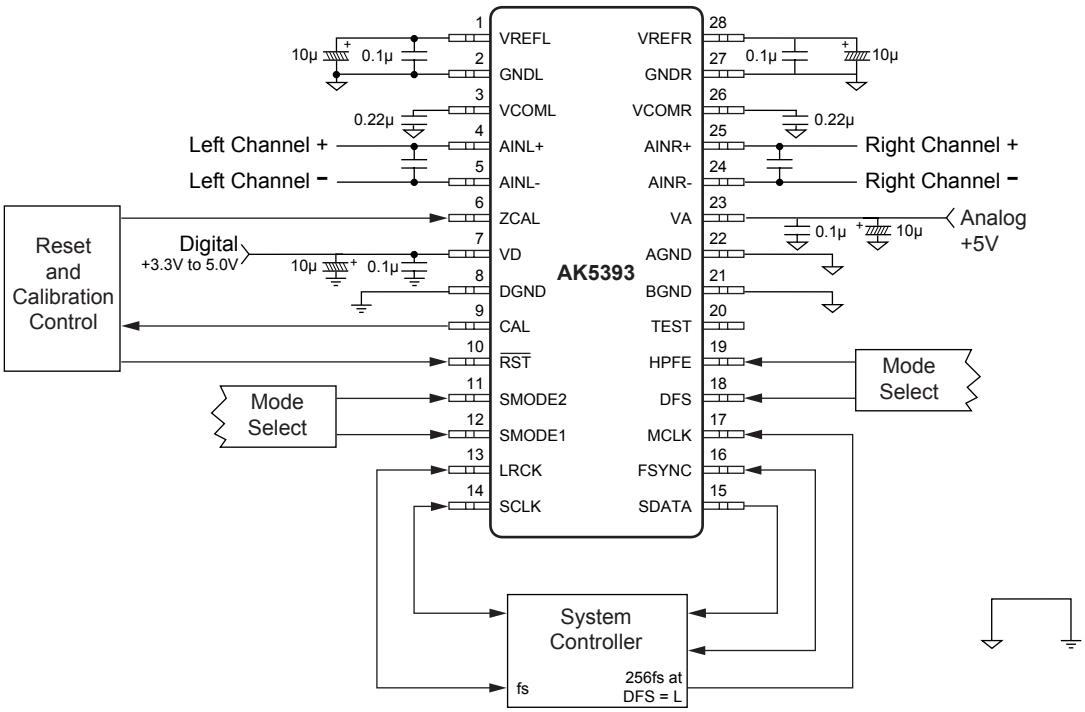


Figure 10. Typical Connection Diagram for Crystal Mode

Grounding and Power Supply Decoupling

Careful attention should be observed for the power supply and grounding of the AK5393. The system's analog and digital grounds are kept separate, but they should be connected together close to where the supplies are brought together into the printed circuit board. The decoupling capacitors should be as close to the AK5393 as possible, with the smaller valued ceramic capacitor being the one nearest to the device.

Voltage Reference and Common Voltage

The AK5393 reference voltage is a differential voltage between the output voltage reference pins (VREFL and VREFR) and the ground pins (GNDL and GNDR). The GNDL and GNDR pins are connected to AGND. In addition, 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor should be connected between the VREFL and GNDL, and between the VREFR and GNDR pins to eliminate the effects of high-frequency noise. It is especially important to place the ceramic capacitors as close to the pins as possible.

All digital signals, especially the clocks, should be kept away from the VREFL and VREFR pins to avoid unwanted coupling with the AK5393. No load current may be drawn from these pins.

The VCOML and VCOMR pins are the common voltages of the analog signals. To eliminate the effects of high-frequency noise, a 0.22µF ceramic capacitor should be connected as close to each of these pins as possible. All signals, especially the clocks, should be kept away from the VCOML and VCOMR pins to avoid unwanted noise coupled into the AK5393. No load current may be drawn from these pins.

Analog Inputs

The AK5393 receives analog signals differentially into the modulator through the analog input pins (AINL-, AINL+, AINR-, and AINR+). Each pin full scale is typically $\pm 2.45V_{P-P}$. The AK5393 can accept input voltages from AGND to VA (that is, from 0V to 5V). The ADC output data is 2's complement. The 24-bit output code is 7FFFFFH for an input signal above a positive full scale, and 800000H for an input signal below a negative full scale. With no input signal, the ideal 24-bit code is 000000H. The DC offset is removed during the offset calibration, or by the HPF in the AK5393.

Internally, the AK5393 samples the analog input signal at 128fs (that is, 6.144MHz at fs = 48kHz when the DFS pin is Low). The digital filter rejects noise above the stop band, except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs so that most audio signals do not have significant energy at 128fs.

The AK5393 accepts +5V voltage supply. The following conditions should be avoided:

- Any voltage above VA + 0.3V
- Any voltage below AGND - 0.3V
- Any current beyond 10mA for the analog input pins.

Caution:
Excessive currents to the input pins may damage the device. Protect input pins from signals at or beyond the limits stated above, especially if using ±15V in other analog circuits.

Figure 11 shows a fully differential input buffer circuit example with an inverted amplifier (gain = -10dB). The 22nF capacitor between AINL-/AINR- and AINL+/AINR+ decreases the feed through noise of the modulator. The 51Ω resistor has been inserted to stabilize the op-amps before the ADC. This circuit acts also as a LPF with a cut-off frequency of about 140kHz. In this example, the internal offset is removed by self calibration. Refer to the evaluation board data sheet for complete details.

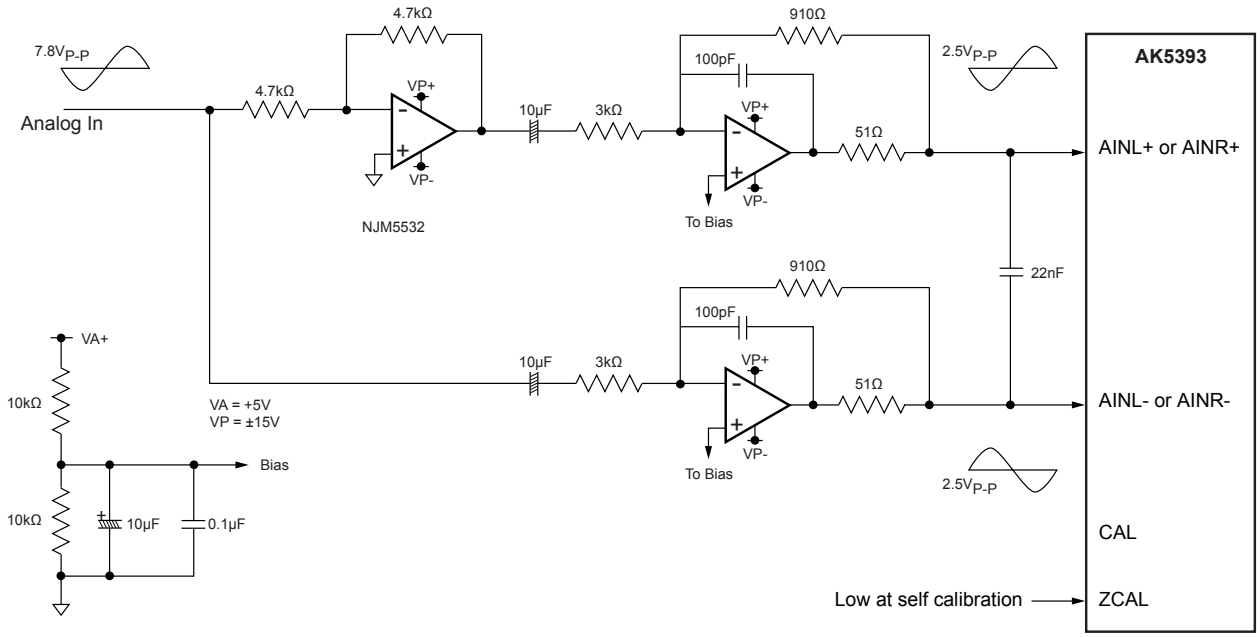


Figure 11. Example of a Differential Input Buffer Circuit

Notes:

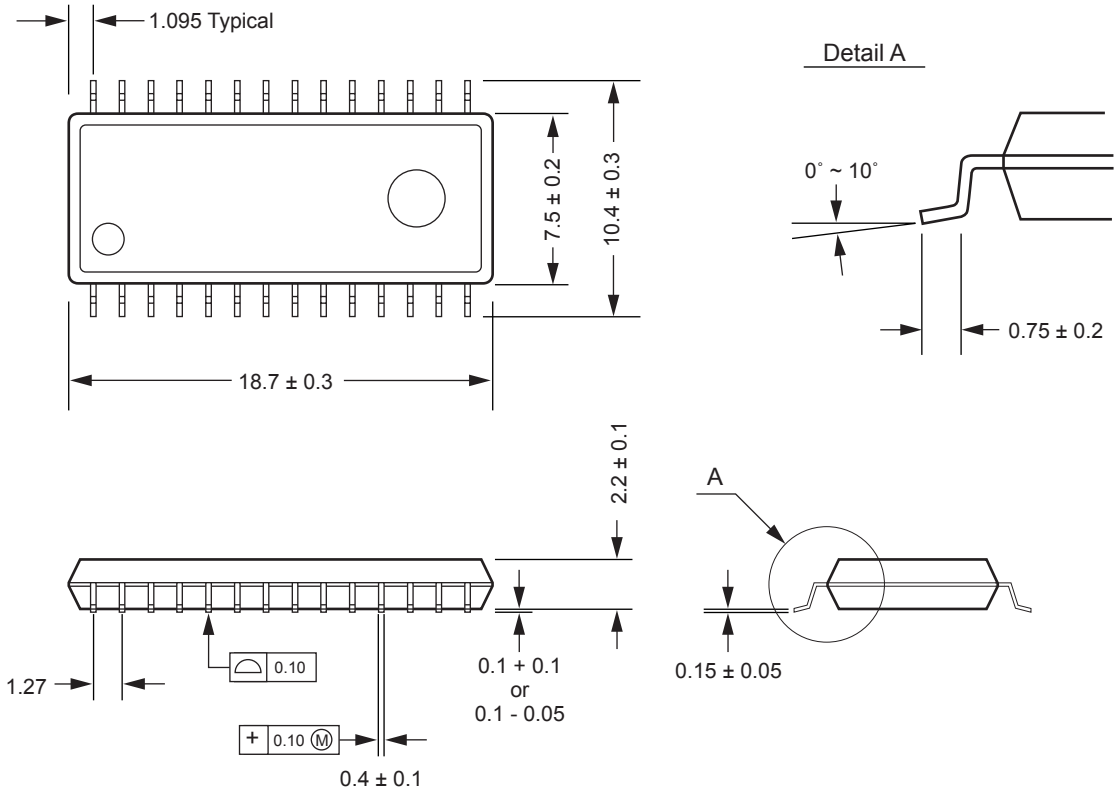
Notes:

Notes:

Package Dimensions

28-Pin SOP

Units: mm



Material and Lead Frame Material:

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder Plate

Package Markings

XXXBYYYYC: Data Code Identifier

XXXB: Lot Number (X: Digit Number, B: Alpha Character)
YYYYC: Assembly Date (YYYY: Digit Number, C: Alpha Character)

Ordering Information

Part Number	Temperature Range	Package
AK5393VS	-10˚C to +70˚C	28-Pin SOP
AKD5393		Evaluation Board