CD54/74HC4059

High-Speed CMOS Logic
CMOS Programmable Divide-by-N Counter

Features

• Synchronous Programmable \( \div N \) Counter \( N = 3 \) to 9999 or 15999
• Presettable Down-Counter
• Fully Static Operation
• Mode-Select Control of Initial Decade Counting Function (\( \div 10, 8, 5, 4, 2 \))
• Master Preset Initialization
• Latchable \( \div N \) Output
• Fanout (Over Temperature Range)
  - Standard Outputs  
  - Bus Driver Outputs
• Wide Operating Temperature Range  
  -55°C to 125°C
• Balanced Propagation Delay and Transition Times
• Significant Power Reduction Compared to LSTTL Logic ICs
• HC Types
  - 2V to 6V Operation
  - High Noise Immunity: \( N_{IL} = 30\% \), \( N_{IH} = 30\% \) of \( V_{CC} \) at \( V_{CC} = 5V \)

Applications

• Communications Digital Frequency Synthesizers; VHF, UHF, FM, AM, etc.
• Fixed or Programmable Frequency Division
• “Time Out” Timer for Consumer-Application Industrial Controls
• AN6374 “Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners”

Description

The 'HC4059 are high-speed silicon-gate devices that are pin-compatible with the CD4059A devices of the CD4000B series. These devices are divide-by-N down-counters that can be programmed to divide an input frequency by any number \( N \) from 3 to 15,999. The output signal is a pulse one clock cycle wide occurring at a rate equal to the input frequency divide by \( N \). The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs \( K_A \), \( K_B \) and \( K_C \) determine the modulus (“divide-by” number) of the first and last counting sections in accordance with the truth table. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section an the last counting section, which consists of flip-flops that are not needed for opening the first counting section. For example, in the \( \div 2 \) mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If \( \div 10 \) is desired for the first section, \( K_A \) is set “high”, \( K_B \) “high” and \( K_C \) “low”. Jam inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade \( \div 10 \) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25 or 50 parts. These inputs set the maximum value of \( N \) at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counter can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the \( \div N \) mode. For example, in the \( \div 8 \) mode, the number from which counting down begins can be preset to:

| 3rd Decade | 1500 |
| 2nd Decade | 150 |
| 1st Decade | 15  |
| Last Counting Section | 1000 |

The total of these numbers (2665) times 8 equals 12,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the \( \div 8 \) mode.

The highest count of the various modes is shown in the Extended Counter Range column. Control inputs \( K_B \) and \( K_C \) can be used to initiate and lock the counter in the “master preset” state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as \( K_B \) and \( K_C \) both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP. RANGE (^{\circ}C)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD54HC4059F3A</td>
<td>-55 to 125</td>
<td>24 Ld CERDIP</td>
</tr>
<tr>
<td>CD74HC4059E</td>
<td>-55 to 125</td>
<td>24 Ld PDIP</td>
</tr>
</tbody>
</table>

NOTE:
1. Wafer and die is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.
The counter should always be put in the master preset mode before the \( \div 5 \) mode is selected. Whenever the master preset mode is used, control signals \( K_b = \text{"low"} \) and \( K_c = \text{"low"} \) must be applied for at least 3 full clock pulses.

After Preset Mode inputs have been changed to one of the \( \div \) modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Figure 1 illustrates a total count of 3 (\( \div 8 \) mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used, the counter jumps back to the “Jam” count when the output pulse appears.

A “high” on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to “low”. If the Latch Enable is “low”, the output pulse will remain high for only one cycle of the clock-input signal.

### Functional Diagram

\[
Q = \left( \frac{f_{IN}}{N} \right)
\]

### Truth Table

<table>
<thead>
<tr>
<th>MODE SELECT INPUT</th>
<th>FIRST COUNTING SECTION</th>
<th>LAST COUNTING SECTION</th>
<th>COUNTER RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( K_a )</td>
<td>( K_b )</td>
<td>( K_c )</td>
<td>CAN BE PRESET TO A MAX OF:</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>2</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>4</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>4 (Note 4)</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>8</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>10</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>L</td>
<td>Master Preset</td>
</tr>
</tbody>
</table>

**NOTES:**

2. \( X = \text{Don't Care} \)

3. \( J1 = \text{Least Significant Bit. J4 = Most Significant Bit.} \)

4. Operation in the \( \div 5 \) mode (1st counting section) requires going through the Master Preset mode prior to going into the \( \div 5 \) mode. At power turn-on, \( K_c \) must be “low” for a period of 3 input clock pulses after \( V_{CC} \) reaches a minimum of 3V.
How to Preset the HC/HCT4059 to Desired \( N \)

The value \( N \) is determined as follows:

\[
N = (\text{MODE}^\dagger) (1000 \times \text{Decade 5 Preset} + 100 \times \text{Decade 4 Preset} + 10 \times \text{Decade 3 Preset} + 1 \times \text{Decade 2 Preset}) + \text{Decade 1 Preset}
\]

\( \dagger \) MODE = First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any \( N \) count, divide the \( N \) count by the Mode. The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

\[
\text{Preset Value} = \frac{N}{\text{Mode}}
\]

Example:

\[
N = 8479, \text{ Mode} = 5
\]

\[
\begin{align*}
1695 + 4 &= \text{Preset Values} \\
5 &\,|\, 8479 \\
\end{align*}
\]

\[\text{Mode Select} = 5\]

\[K_a, K_b, K_c\]

\[\text{J1 J2 J3 J4} \quad L \quad L \quad H \quad H \]
\[\text{J5 J6 J7 J8} \quad H \quad L \quad H \quad L \]
\[\text{J9 J10 J11 J12} \quad H \quad L \quad L \quad H \]
\[\text{J13 J14 J15 J16} \quad L \quad H \quad H \quad L \]

NOTE:

To verify the results, use Equation 1:

\[
N = 5 (1000 \times 1 + 100 \times 6 + 10 \times 9 + 1 \times 5) + 4
\]

\[
N = 8479
\]

**Program Jam Inputs (BCD)**

**Program Jam Inputs (BCD)**
### Absolute Maximum Ratings

- **DC Supply Voltage, \( V_{CC} \):** -0.5V to 7V
- **DC Input Diode Current, \( I_{IK} \):**
  - For \( V_I < -0.5V \) or \( V_I > V_{CC} + 0.5V \): ±20mA
- **DC Output Diode Current, \( I_{OK} \):**
  - For \( V_O < -0.5V \) or \( V_O > V_{CC} + 0.5V \): ±20mA
- **DC Output Source or Sink Current per Output Pin, \( I_O \):**
  - For \( V_O > -0.5V \) or \( V_O < V_{CC} + 0.5V \): ±25mA
- **DC \( V_{CC} \) or Ground Current, \( I_{CC} \):** ±50mA

### Operating Conditions

- **Temperature Range, \( T_A \):** -55°C to 125°C
- **Supply Voltage Range, \( V_{CC} \):** 2V to 6V
- **DC Input or Output Voltage, \( V_I, V_O \):** 0V to \( V_{CC} \)
- **Input Rise and Fall Time:**
  - 2V: 1000ns (Max)
  - 4.5V: 500ns (Max)
  - 6V: 400ns (Max)

### Thermal Information

- **PDIP Package:** 60°C/W
- **Maximum Junction Temperature (Hermetic Package or Die):** 175°C
- **Maximum Junction Temperature (Plastic Package):** 150°C
- **Maximum Storage Temperature Range:** -65°C to 150°C
- **Maximum Lead Temperature (Soldering 10s):** 300°C

### CAUTION:

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### DC Electrical Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} ) (V)</th>
<th>25°C</th>
<th>-40°C TO 85°C</th>
<th>-55°C TO 125°C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>High Level Input Voltage</td>
<td>( V_{IH} )</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>1.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Low Level Input Voltage</td>
<td>( V_{IL} )</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>High Level Output Voltage CMOS Loads</td>
<td>( V_{OH} )</td>
<td>( V_{IH} ) or ( V_{IL} )</td>
<td>-0.02</td>
<td>2</td>
<td>1.9</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>High Level Output Voltage TTL Loads</td>
<td>( V_{OL} )</td>
<td>( V_{IH} ) or ( V_{IL} )</td>
<td>-0.02</td>
<td>4.5</td>
<td>4.4</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>( I_I )</td>
<td>( V_{CC} ) or GND</td>
<td>-</td>
<td>6</td>
<td>±0.1</td>
<td>-</td>
<td>±1</td>
</tr>
<tr>
<td>Quiescent Device Current</td>
<td>( I_{CC} )</td>
<td>( V_{CC} ) or GND</td>
<td>0</td>
<td>6</td>
<td>8</td>
<td>-</td>
<td>80</td>
</tr>
</tbody>
</table>
## Prerequisite for Switching Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>V\text{CC} (V)</th>
<th>25\degree\text{C}</th>
<th>-40\degree\text{C} TO 85\degree\text{C}</th>
<th>-55\degree\text{C} TO 125\degree\text{C}</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>Pulse Width CP</td>
<td>\text{t}_W</td>
<td>2</td>
<td>90</td>
<td>-</td>
<td>-</td>
<td>115</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>18</td>
<td>-</td>
<td>-</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Setup Time</td>
<td>\text{t}_{SU}</td>
<td>2</td>
<td>75</td>
<td>-</td>
<td>-</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>13</td>
<td>-</td>
<td>-</td>
<td>16</td>
</tr>
<tr>
<td>CP Frequency</td>
<td>\text{f}_{\text{MAX}}</td>
<td>2</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5</td>
<td>27</td>
<td>-</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>32</td>
<td>-</td>
<td>-</td>
<td>26</td>
</tr>
</tbody>
</table>

## Switching Specifications

Input \( t_r, t_f = 6\,\text{ns} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>V\text{CC} (V)</th>
<th>25\degree\text{C}</th>
<th>-40\degree\text{C} TO 85\degree\text{C}</th>
<th>-55\degree\text{C} TO 125\degree\text{C}</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>\text{t}<em>{\text{PLH}}, \text{t}</em>{\text{PHL}}</td>
<td>\text{C}_L = 50\text{pF}</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>-</td>
<td>-</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{C}_L = 15\text{pF}</td>
<td>5</td>
<td>-</td>
<td>17</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{C}_L = 15\text{pF}</td>
<td>4.5</td>
<td>-</td>
<td>35</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>-</td>
<td>30</td>
<td>-</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>\text{t}<em>{\text{PLH}}, \text{t}</em>{\text{PHL}}</td>
<td>\text{C}_L = 50\text{pF}</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>175</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td>-</td>
<td>-</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{C}_L = 15\text{pF}</td>
<td>5</td>
<td>-</td>
<td>14</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output Transition Time</td>
<td>\text{t}<em>{\text{THL}}, \text{t}</em>{\text{TLH}}</td>
<td>\text{C}_L = 50\text{pF}</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td>-</td>
<td>-</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>-</td>
<td>13</td>
<td>-</td>
</tr>
<tr>
<td>CP Frequency</td>
<td>\text{f}_{\text{MAX}}</td>
<td>\text{C}_L = 15\text{pF}</td>
<td>5</td>
<td>-</td>
<td>54</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>\text{C}_I</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Power Dissipation Capacity</td>
<td>\text{C}_{\text{PD}}</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>36</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**NOTES:**

6. \( \text{C}_{\text{PD}} \) is used to determine the dynamic power consumption, per package.

7. \( P_D = C_{\text{PD}} V_{\text{CC}}^2 f_i + \Sigma C_L V_{\text{CC}}^2 f_o \) where \( f_i \) = input frequency, \( f_o \) = output frequency, \( C_L \) = output load capacitance, \( V_{\text{CC}} \) = supply voltage.
Test Circuits and Waveforms

NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

**FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

**FIGURE 4. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer’s applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI’s publication of information regarding any third party’s products or services does not constitute TI’s approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated