DATA SHEET

凌陽科技
SUNPLUS

SPLB31A

2368 Dots Data Bank

Preliminary

JUL. 24, 2001

Version 0.3

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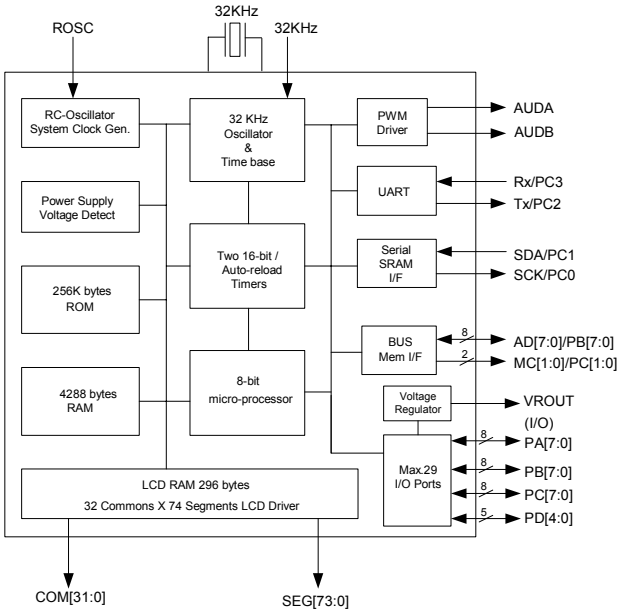
2368 DOTS DATA BANK

1. GENERAL DESCRIPTION

The SPLB31A, an 8-bit CMOS microprocessor, contains 4288 bytes working RAM, 256K bytes ROM, 14 I/Os, interrupt/wakeup controller, UART for serial communication, Serial SRAM interface and Bus memory interface for memory expansion, and automatic display controller/driver for LCD. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data (speech duration is approx. 69 seconds at a 7KHz sampling rate using a 4-bit ADPCM). The built-in UART speeds up data transmission between two devices. Furthermore, a SLEEP (power-down) function is also built in to extend power life. The SPLB31A is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. BLOCK DIAGRAM



Note1: PA[3:7] share pins with SEG[73:69] (mask option).
Note2: PB[7:0] share pins with Bus memory interface Addr/Data bus.
Note3: PC[1:0] share pins with Bus memory interface MC[1:0]. Also share pins with Serial SRAM interface SDA/SCK.
Note4: PC[3:2] share pins with UART Rx/Tx.
Note5: PC[4:7] share pins with SEG[68:65] (mask option).
Note6: PD[0:4] share pins with COM[31:27] (mask option).

3. FEATURES

- Built-in 8-bit processor
  - **4288 bytes SRAM**
  - **256K bytes ROM**
  - Max. operating speed: 4.0MHz @ 2.4V - 3.6V
    5.0MHz @ 3.6V - 5.5V
  - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
  - Provides 6 wake-up sources
  - Provides 7 interrupt sources
- Asynchronous serial interface (UART)
- Serial SRAM interface
- Bus memory interface
- Built-in voltage regulator for external memory devices
- Key scan function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
  - **Up to 74 segments, up to 32 commons, maximum 2368 dots**
  - 1/5, 1/6 bias; 1/32 duty capability
  - **296 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control
- Power saving SLEEP mode
- **Low voltage detector**
  - **8-level 2.9V - 2.2V/4.35V - 3.3V detection**
  - **2.2V Low voltage reset**
- Wide operating voltage range:
  - 2.4V - 3.6V
  - 3.6V - 5.5V
- Peripherals
  - **Max. 29 I/O pins (PA[7:0], PB[7:0], PC[7:0], PD[4:0])**
    . Dedicated I/Os: PA[2:0]
    . Shared pin I/Os:
    PA[3:7]/SEG[73:69]
    PB[7:0]/BMI AD Bus [7:0]
    PC[1:0]/BMI MC[1:0]/SSRAM SDA, SCK
    PC[3:2]/UART Tx/Rx
    PC[4:7]/SEG[68:65]
    PD[0:4]/COM[31:27]
  - 32.768KHz oscillator circuit for RTC
  - RC-oscillator (only one resistor is needed)
  - Two 16-bit reloadable timer/counters
  - **8-bit DAC resolution, 2-channel PWM audio outputs**
  - Watchdog Timer for reliable operation

■ Low-power consumption:
- 600μA typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC}=4.0MHz
- 25μA typical halt current @ 3.0V
- <1μA typical standby current @ 3.0V

4. APPICATION FIELD

■ Hand held games
■ Scientific calculator
■ Talking calculator, Talking clock
■ Talking instrument controller
■ General speech synthesizer
■ Data Bank

5. SIGNAL DESCRIPTIONS

Total: 142 pins

Mnemonic	PIN No.	Type	Description
SEG24 - 0 SEG64 - 25 SEG68 - 65 / PC4 - 7 SEG73 - 69 / PA3 - 7	1 - 25 103 - 142 99 - 102 94 - 98	O	LCD driver segment output. SEG15 - 0 share pin with key scan port. SEG68 - 65 optioned to PC4 - 7. SEG73 - 69 optioned to PA3 - 7.
COM15 - 0 COM26 - 16 COM31 - 27 / PD0 - 4	24 - 41 88 - 78 93 - 89	O	LCD driver common output. COM31 - 27 can be optioned to PD0 - 4.
PA2 - 0	58 - 60	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PB7 - 0	50 - 57	I/O	Port B is a bi-directional I/O port. Share pin with Bus Memory Interface Addr/Data
PC1 / MC1 / SDA PC0 / MC0 / SCK	48 49	I/O	Port C is a bi-directional I/O port. Share pin with Bus Memory MC1 - 0. Also share pin with SDA/SCK.
PC3 / Rx	46	I/O	UART input. Share pin with PC3.
PC2 / Tx	47	I/O	UART output. Share pin with PC2.
ROSC	62	I	ROSC input, connect to VDD through a resistor
$\overline{\text{RESET}}$	66	I	System reset input, low active.
AUDA, AUDB	45, 43	O	PWM audio output
X32I	65	I	32.768KHz crystal input or connect to VDD through a resistor (option).
X32O	64	O	32.768KHz crystal output
TEST	63	I	Test input
CUP4 - 1	72 - 69	P	LCD voltage generation. Charge pump capacitor interconnection pins
VLCD	77	P	LCD voltage generation.
V4 - 1	76 - 73	P	LCD voltage generation.
VROUT	68	P	Internal regulator output. Enable or disable via bonding option. Should be connected to VDD if internal Regulator is disabled.
VDD	67	P	Power supply voltage input
VSS	61	P	Ground reference
PVDD	44	P	PWM driver power
PVSS	42	P	PWM driver ground reference
BOPT1 - 0	67A, 44A	B	Internal regulator output voltage select option pin (internally pull-low)*
BOPT2	61A	B	Internal regulator enable/disable option pin (internally pull-high)*

Legend: I = Input, O = Output, P = Power, B = Bonding option

Note: *See bonding option section for details.

6. FUNCTIONAL DESCRIPTIONS

6.1. Memories

The SPLB31A contains 256K-byte ROM and 4288-byte SRAM. Cooperating with Sunplus bus extender, SPBA01A, the external memory, either RAM or ROM, can be extended up to 4MB. Serial SRAM interface is also provided in SPLB31A, thus SRAM space can be extended by using Sunplus Serial SRAM, SPRS512C or SPRS1024C.

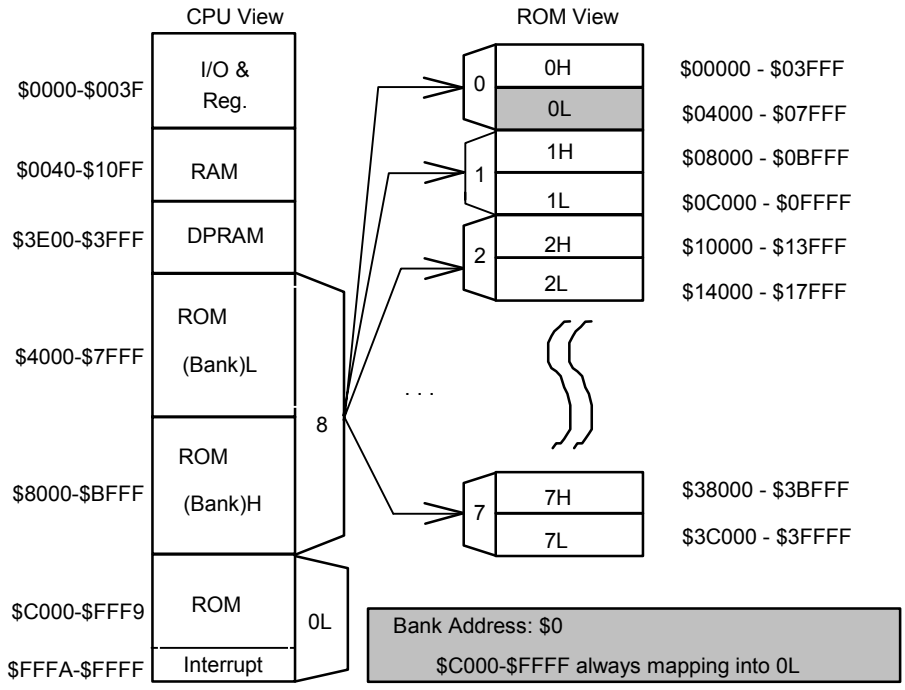
6.2. Map of Memory and I/Os

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



1. $4000-$BFFF can be external memory if MEXT ($07.7) = 1 and Bank port ($00.7) = 1.
2. $C000-$FFFF can be external memory if MEXT ($07.7) = 1 and EXC($0b.1) = 1.
3. User program should start from $C800. $C000-$C7FF is the test program area.
4. User program interrupt vector: $FFFA ~ $FFFF
5. Test program interrupt vector: $FFF2 ~ $FFF7

6.3. Operating States

There are three operation modes involved in SPLB31A: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest current.

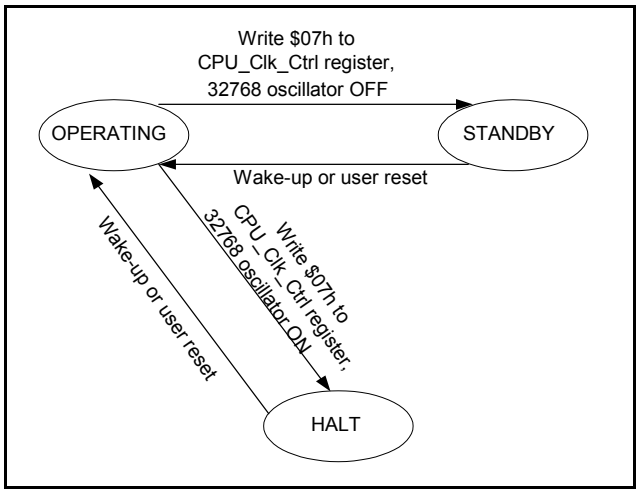
6.3.2. Standby mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) and turn off 32768Hz oscillator to activate standby mode. The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.3.3. Halt mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the SPLB31A state diagram:



SPLB31A State Diagram

6.4. Speech and Melody

For speech synthesis, the SPLB31A provides several timer interrupts for a precise sampling frequency. The sound data can be stored into ROM and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the SPLB31A provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

The SPLB31A contains a 2368-dot LCD controller/driver. Programmers is able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in SPLB31A supports 1/16 - 1/32 duty and 1/5 - 1/6 bias.

6.6. LCD Voltage Generation

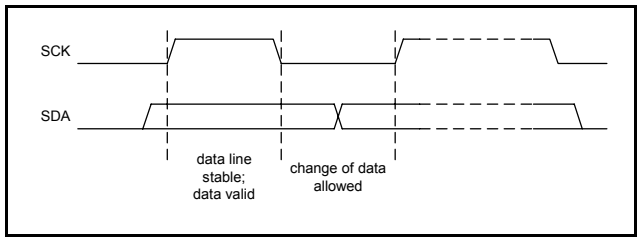
The SPLB31A offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage (V2) for the charge-pumping circuit to generate VLCD. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 2.45V to 5.75V (in 1/5 LCD bias) or 2.95V to 6.85V (in 1/6 LCD bias) with 32 levels.

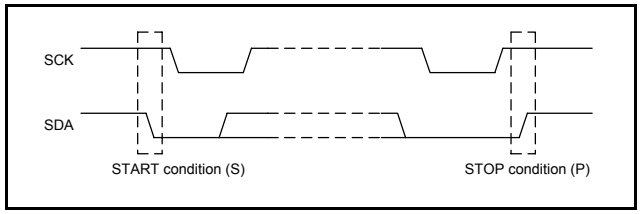
6.7. PWM Output

Internally, the SPLB31A has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

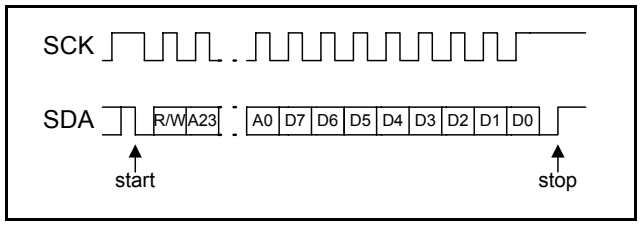
6.8. Serial SRAM Interface

The Serial SRAM interface is able to expand the data storage SRAM. The Control Registers are ranged from $30-$36. Note that The pins of SDA and SCK are shared with PC [1:0] and therefore, users should set PC[1:0] as Serial SRAM interface by writing to Port $27[1:0].

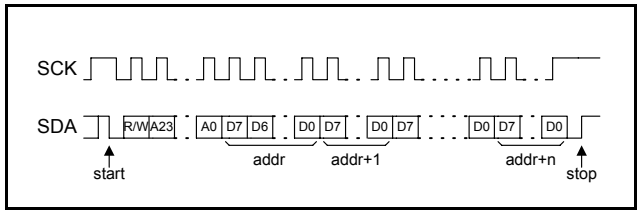




6.8.1. Read/Write timing



6.8.2. Continuous Read/Write timing



6.9. Bus Memory Interface

A built-in Bus memory interface is available on SPLB31A. Through the use of Bus memory interface, user can expand the memory space by using a external Bus memory (SRAM, mask ROM or Flash). The Bus memory interface includes 10 signal pins: MC1, MC0 and AD BUS[7:0] which shared pad with port B. Before using

the Bus memory interface, users should set MEXT=1 ($03.7) and BANK register ($0), then access address $4000-BFFF to read or write data from external bus memory. Note that when using Bus memory interface, CPU clock setting can not be set as F_{OSC}/1, should be /2 or slower.

MC1	MC0	AD BUS [7:0]
L	L	Data for Write
L	H	Data for Read
H	L	AL (Address Low byte)
H	H	AH (Address High byte)

6.10. Voltage Regulator

The SPLB31A offers a voltage regulator, which supplies power source for external memory devices. The voltage regulator can output four voltage levels, 2.5V/2.6V/2.7V/3.0V via bonding option. The output voltage level should be properly selected based on the electrical characteristics of external memory devices involved.

6.11. Asynchronous Serial Interface (UART)

The SPLB31A supports a 1-channel UART for serial communications. The bit-rate is up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be configured in the command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. Reading the status register informs whether the interrupt is generated by Rx or Tx. Frame, overrun and parity errors are detected as each byte is received and all error status can be read from status register.

The UART supports clock auto calibration. If auto calibration is selected, standard baud rate from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to the baud rate control registers. The supported baud rates and their minimum R-oscillator clock frequency requirements are shown in the table below.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained by this method. In the non-calibration mode, users should understand that the R-oscillator frequency may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.12. Low Voltage Detection

The SPLB31A provides an 8-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V.

6.13. Watchdog Timer (WDT)

An on chip watchdog timer is also available in the SPLB31A. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared every 0.5 second to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.14. Mask Options

6.14.1. 32768 oscillator

1). X'TAL

2). R-oscillator

6.14.2. Watchdog timer

1). Enable

2). Disable

6.14.3. PA[3:7]/SEG[73:69]

Each port/segment can be optioned as I/O or LCD segment output individually.

6.14.4. PC[4:7]/SEG[68:65]

Each port/segment can be optioned as I/O or LCD segment output individually.

6.14.5. PD[0:4]/COM[31:27]

Each port/segment can be optioned as I/O or LCD segment output individually.

6.15. Bonding Options

6.15.1. Voltage regulator

1). Enable

2). Disable

6.15.2. Regulator output selection

1). 2.5V

2). 2.6V

3). 2.7V

4). 3.0V

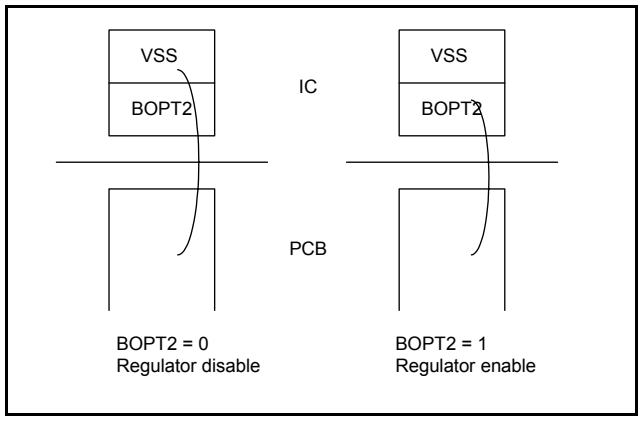


Figure1: Bonding option for regulator Enable/Disable

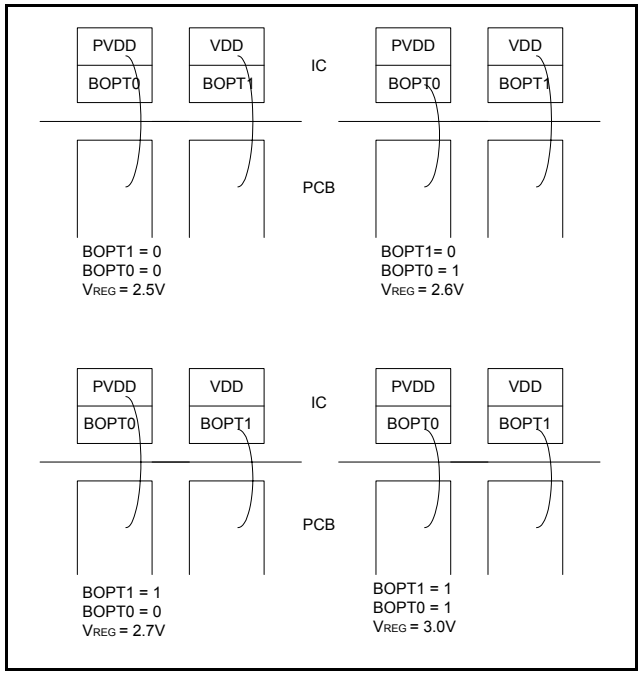


Figure2: Bonding option for regulator output voltage select

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

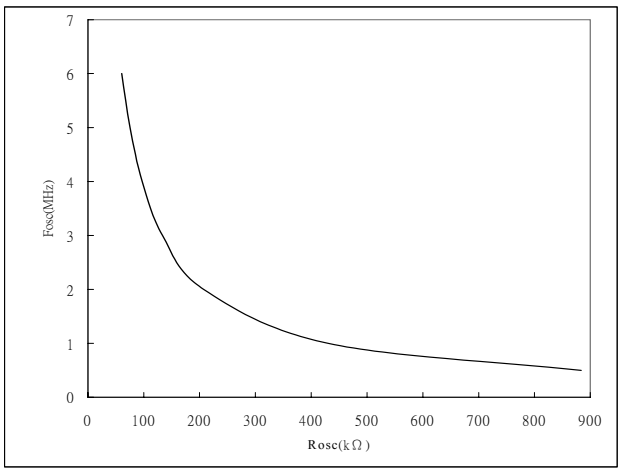
7.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	600	-	μA	F_{CPU} = 1.0MHz @ 3.0V F_{ROSC} = 4.0MHz, no load
Halt Current	I_{HALT}	-	25	-	μA	VDD = 3.0V, 32K X'tal ON, LCD ON, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0			mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
		2.95	-	6.85	V	VDD = 3.0V, 1/6 bias, no load
Regulator Output Voltage	V_{REG}	-	2.5	-	V	Output voltage is selected by bonding option
		-	2.6	-		
		-	2.7	-		
		-	3.0	-		
Regulator output voltage drop	V_{RDROP}	-	-	100	mV	I_L = 1.0mA, VDD = 3.6V
OSC Resistor	R_{OSC}	-	160	-	KΩ	F_{OSC} = 2.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	4.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4V
		-	-	5.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V

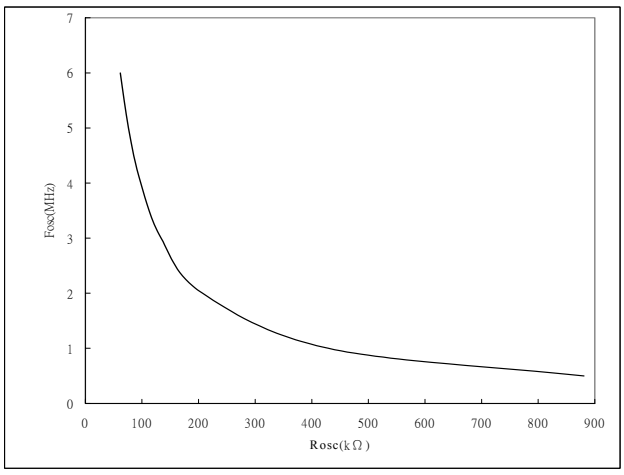
Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. The Relationships between the R_{OSC} and the F_{OSC}

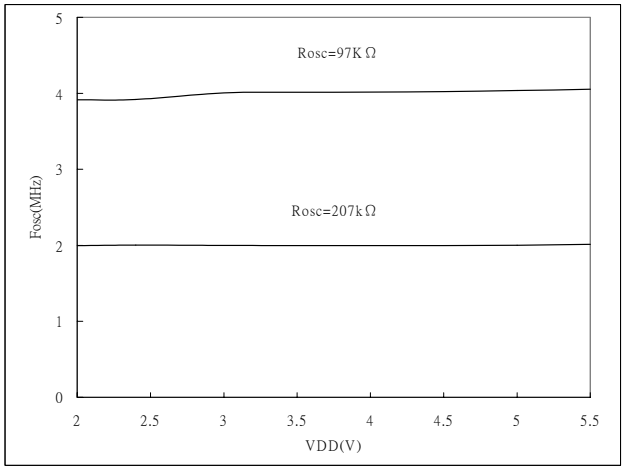
7.3.1. VDD = 3.0V



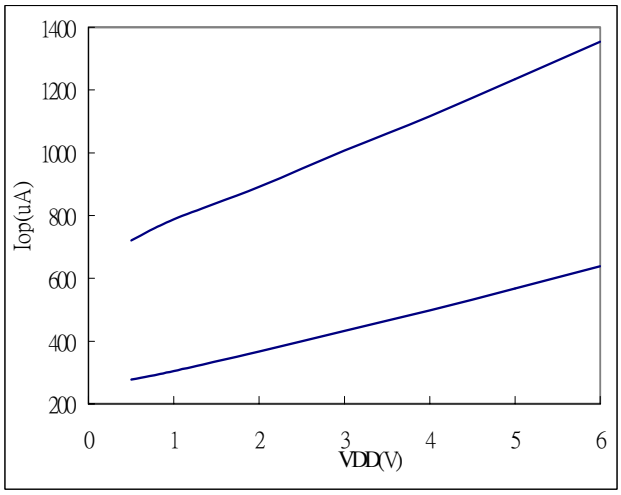
7.3.2. VDD = 4.5V



7.4. The Relationships between the VDD and the F_{OSC}

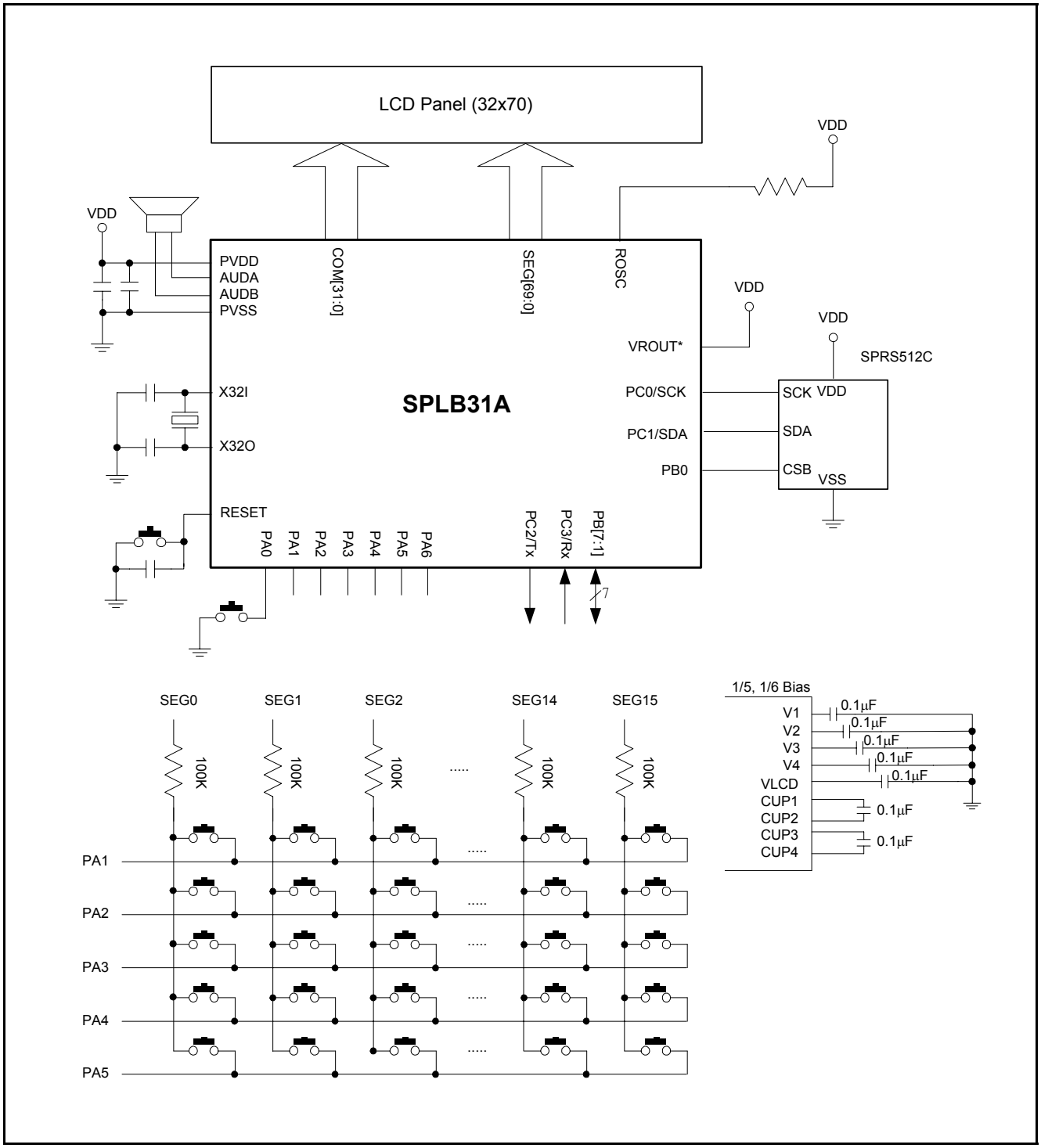


7.5. The Relationships between the F_{OSC} and the I_{OP}



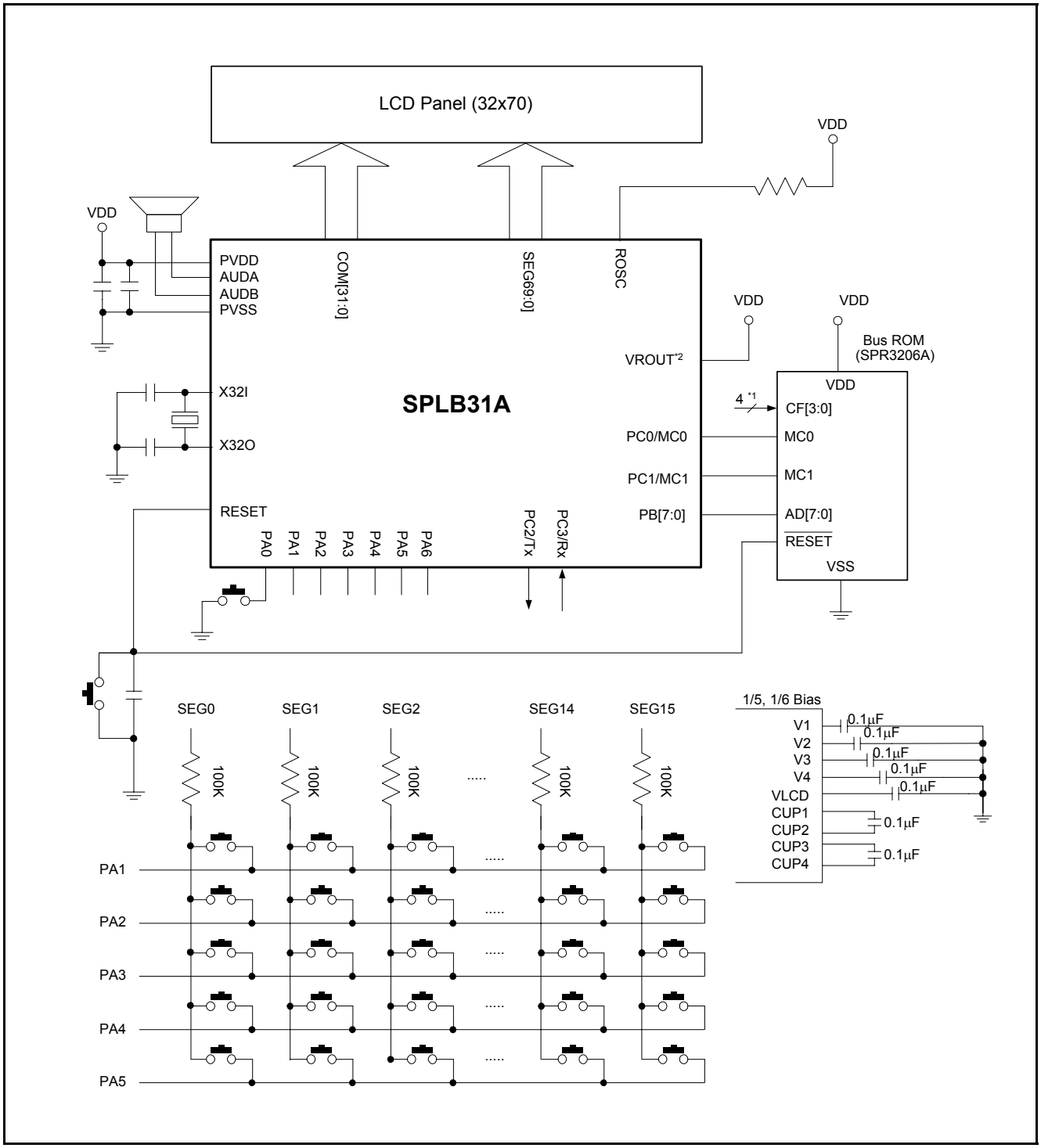
8. APPLICATION CIRCUITS

8.1. 2240 Dots LCD Driver, 70 Segments × 32 Commons with External Serial SRAM, Regulator Disabled - (1)



Note: *Pin VROUT should be connected to VDD if internal Regulator is disabled.

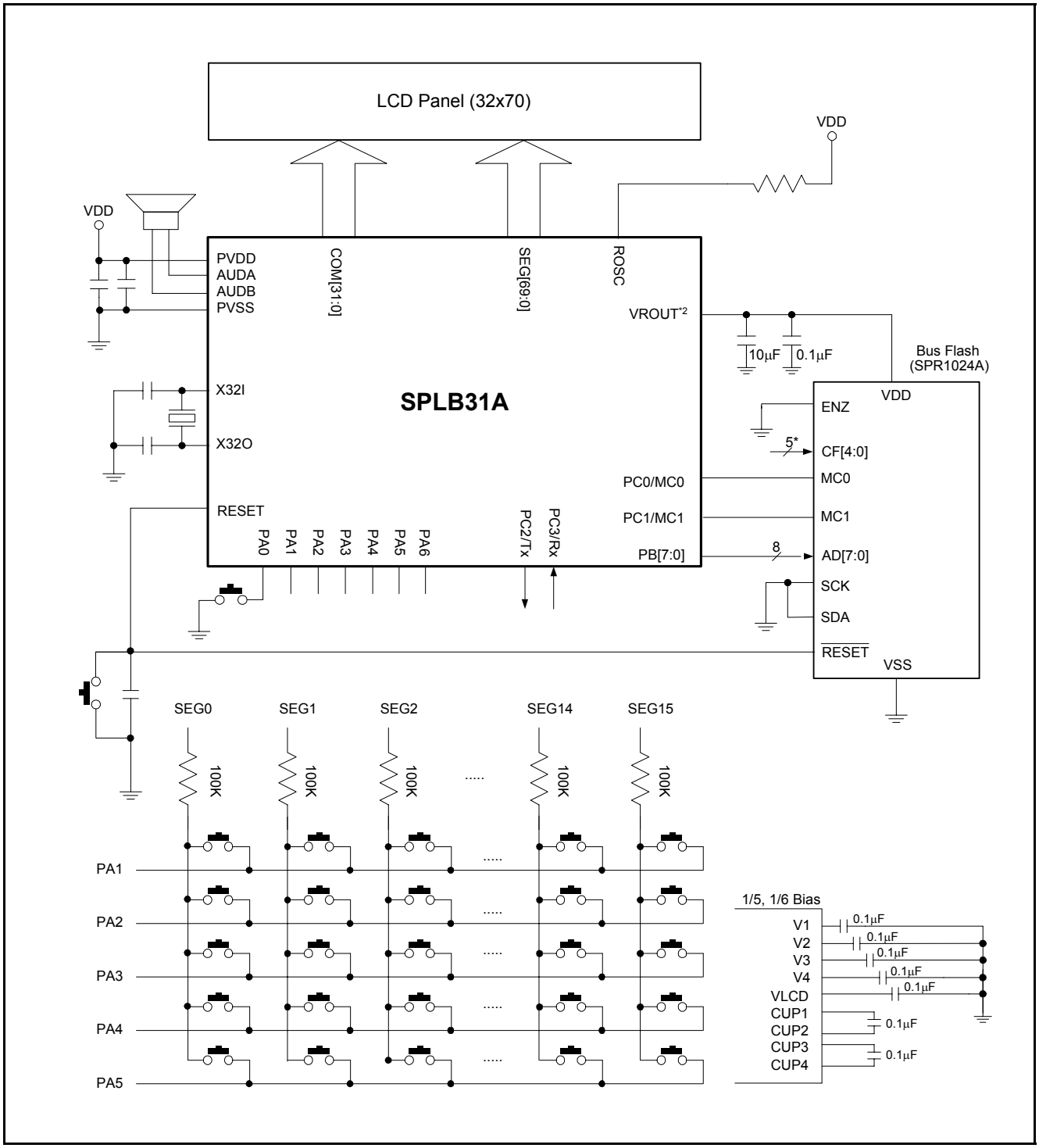
8.2. 2240 Dots LCD Driver, 70 Segments × 32 Commons with External Bus ROM, Regulator Disabled - (2)



Note1: Detail settings of these pins please refer to the data sheet of SPR3206A.

Note2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

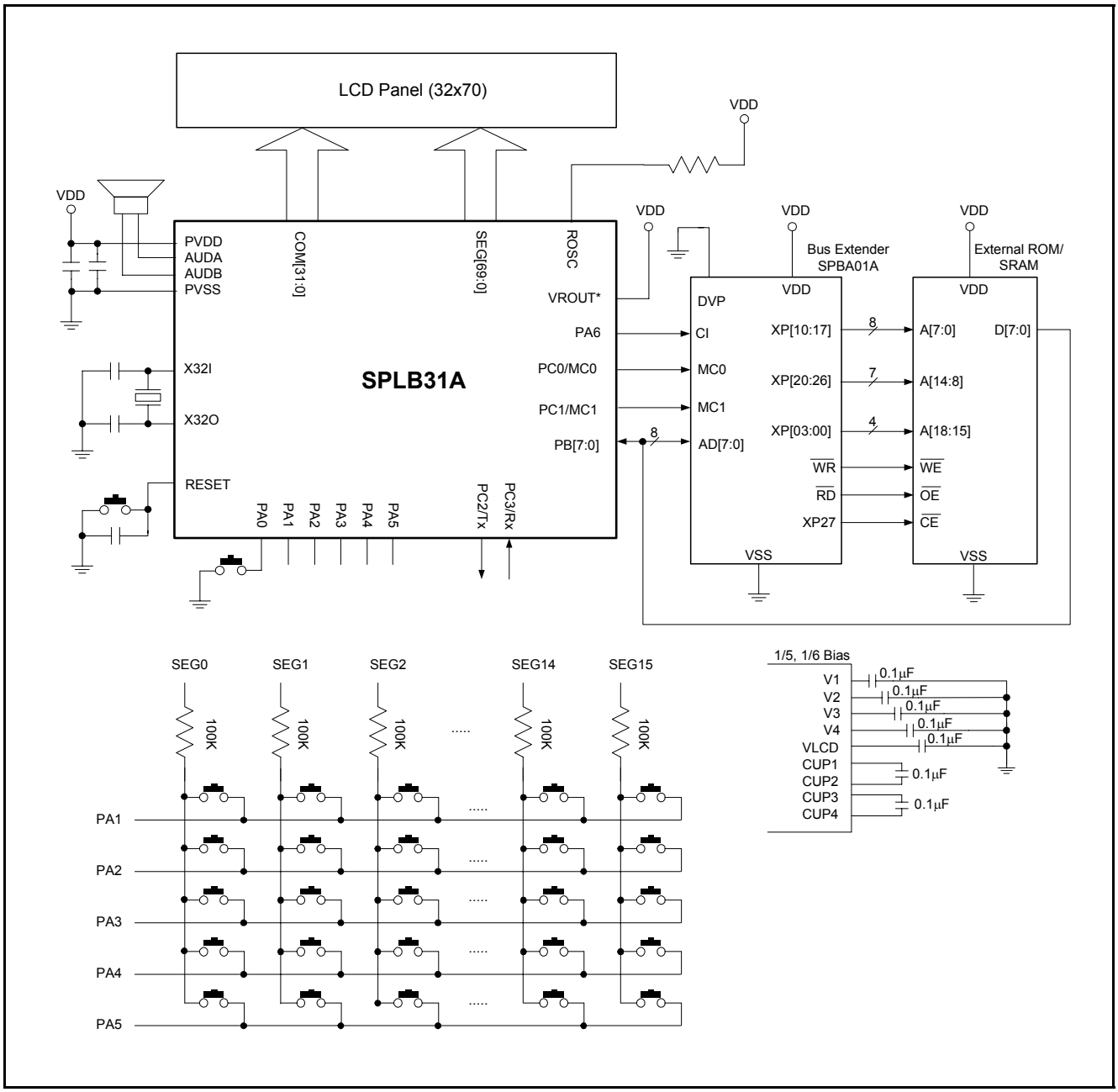
8.3. 2240 Dots LCD Driver, 70 Segments × 32 Commons with External Bus Flash, Regulator Enabled - (3)



Note1: Detail settings of these pins please refer to the data sheet of SPR1024A

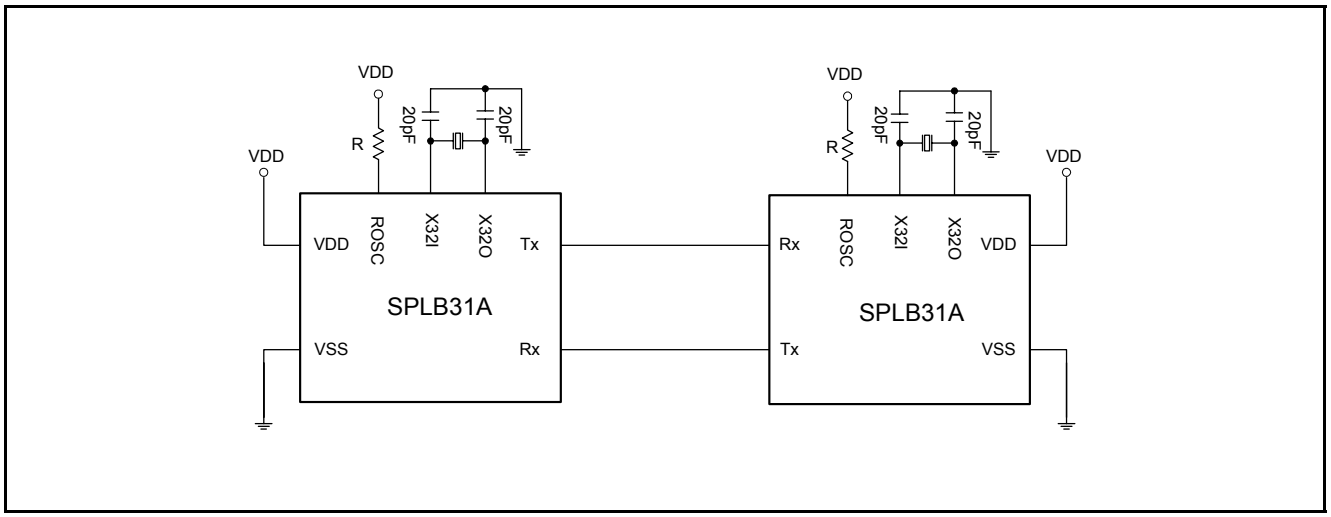
Note2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

8.4. 2240 Dots LCD Driver, 70 Segments × 32 Commons With Bus Extender, Regulator Disabled - (4)



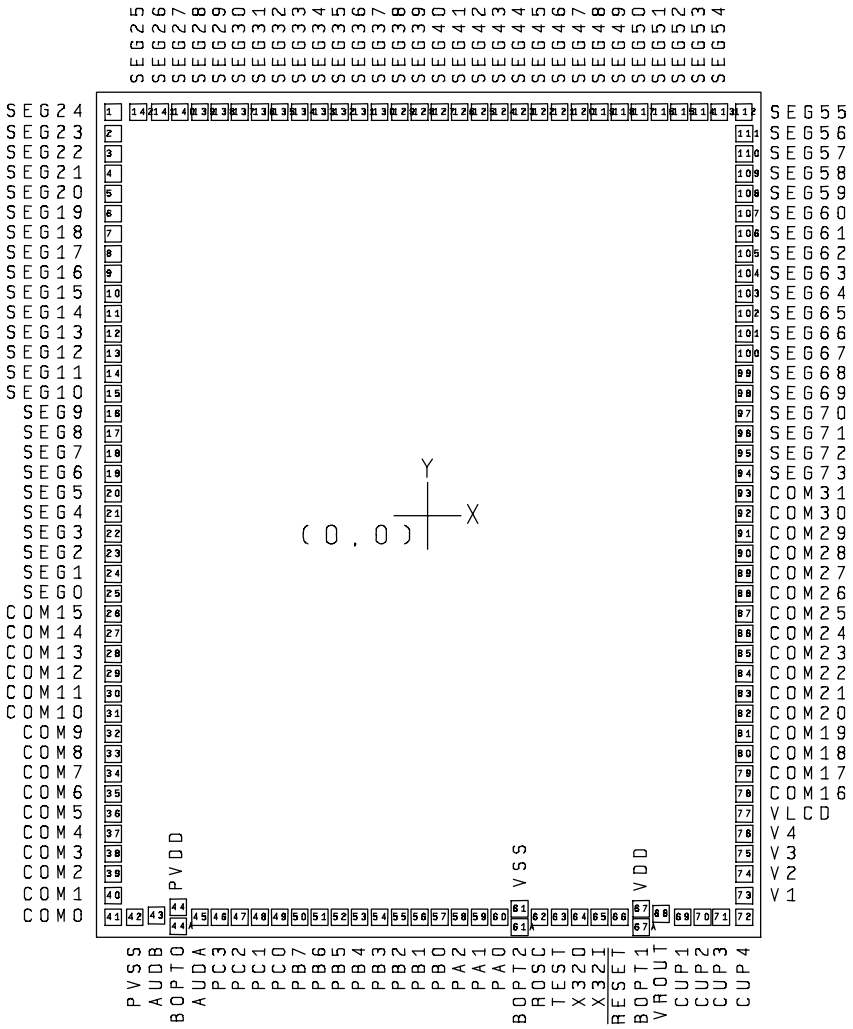
Note: *Pin VROUT should be connected to VDD if internal Regulator is disabled.

8.5. Serial Communications between two SPLB31As - (5)



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 4090μm x 5180μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

Note3: Pin VROUT should be connected to VDD if internal Regulator is disabled.

9.2. Ordering Information

Product Number	Package Type
SPLB31A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG24	-1898	2417	44A	BOPT0	-1508	-2450
2	SEG23	-1898	2282	45	AUDA	-1379	-2413
3	SEG22	-1898	2162	46	PC3	-1259	-2413
4	SEG21	-1898	2042	47	PC2	-1139	-2413
5	SEG20	-1898	1922	48	PC1	-1019	-2413
6	SEG19	-1898	1802	49	PC0	-899	-2413
7	SEG18	-1898	1682	50	PB7	-779	-2413
8	SEG17	-1898	1562	51	PB6	-659	-2413
9	SEG16	-1898	1442	52	PB5	-539	-2413
10	SEG15	-1898	1322	53	PB4	-419	-2413
11	SEG14	-1898	1202	54	PB3	-299	-2413
12	SEG13	-1898	1082	55	PB2	-179	-2413
13	SEG12	-1898	962	56	PB1	-59	-2413
14	SEG11	-1898	842	57	PB0	61	-2413
15	SEG10	-1898	722	58	PA2	181	-2413
16	SEG9	-1898	602	59	PA1	301	-2413
17	SEG8	-1898	482	60	PA0	421	-2413
18	SEG7	-1898	362	61	VSS	541	-2360
19	SEG6	-1898	242	61A	BOPT2	541	-2450
20	SEG5	-1898	122	62	ROSC	661	-2413
21	SEG4	-1898	2	63	TEST	781	-2413
22	SEG3	-1898	-118	64	X32O	901	-2413
23	SEG2	-1898	-238	65	X32I	1021	-2413
24	SEG1	-1898	-358	66	$\overline{\text{RESET}}$	1141	-2413
25	SEG0	-1898	-478	67	VDD	1271	-2360
26	COM15	-1898	-598	67A	BOPT1	1271	-2450
27	COM14	-1898	-718	68	VROUT	1396	-2393
28	COM13	-1898	-838	69	CUP1	1521	-2413
29	COM12	-1898	-958	70	CUP2	1641	-2413
30	COM11	-1898	-1078	71	CUP3	1758	-2413
31	COM10	-1898	-1198	72	CUP4	1891	-2413
32	COM9	-1898	-1318	73	V1	1892	-2283
33	COM8	-1898	-1438	74	V2	1892	-2158
34	COM7	-1898	-1558	75	V3	1892	-2038
35	COM6	-1898	-1678	76	V4	1892	-1919
36	COM5	-1898	-1798	77	VLCD	1891	-1798
37	COM4	-1898	-1918	78	COM16	1891	-1678
38	COM3	-1898	-2038	79	COM17	1891	-1558
39	COM2	-1898	-2158	80	COM18	1891	-1438
40	COM1	-1898	-2283	81	COM19	1891	-1318
41	COM0	-1898	-2413	82	COM20	1891	-1198
42	PVSS	-1768	-2413	83	COM21	1891	-1078
43	AUDB	-1638	-2413	84	COM22	1891	-958
44	PVDD	-1509	-2350	85	COM23	1891	-838

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
86	COM24	1891	-718	115	SEG52	1501	2417
87	COM25	1891	-598	116	SEG51	1381	2417
88	COM26	1891	-478	117	SEG50	1261	2417
89	COM27	1891	-358	118	SEG49	1141	2417
90	COM28	1891	-238	119	SEG48	1021	2417
91	COM29	1891	-118	120	SEG47	901	2417
92	COM30	1891	2	121	SEG46	781	2417
93	COM31	1891	122	122	SEG45	661	2417
94	SEG73	1891	242	123	SEG44	541	2417
95	SEG72	1891	362	124	SEG43	421	2417
96	SEG71	1891	482	125	SEG42	301	2417
97	SEG70	1891	602	126	SEG41	181	2417
98	SEG69	1891	722	127	SEG40	61	2417
99	SEG68	1891	842	128	SEG39	-59	2417
100	SEG67	1891	962	129	SEG38	-179	2417
101	SEG66	1891	1082	130	SEG37	-299	2417
102	SEG65	1891	1202	131	SEG36	-419	2417
103	SEG64	1891	1322	132	SEG35	-539	2417
104	SEG63	1891	1442	133	SEG34	-659	2417
105	SEG62	1891	1562	134	SEG33	-779	2417
106	SEG61	1891	1682	135	SEG32	-899	2417
107	SEG60	1891	1802	136	SEG31	-1019	2417
108	SEG59	1891	1922	137	SEG30	-1139	2417
109	SEG58	1891	2042	138	SEG29	-1259	2417
110	SEG57	1891	2162	139	SEG28	-1379	2417
111	SEG56	1891	2282	140	SEG27	-1499	2417
112	SEG55	1891	2417	141	SEG26	-1619	2417
113	SEG54	1746	2417	142	SEG25	-1744	2417
114	SEG53	1621	2417				

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 08, 2001	0.1	Original	
APR. 19, 2001	0.2	LCD contrast control range (VLCD) in 1/5 bias changed from 3.0V - 7.0V to 2.45V - 5.70V	
JUL. 24, 2001	0.3	1. Correct “Write $0fh to CPU_Clk_Ctrl register” to “Write $07h to CPU_Clk_Ctrl register” in the “*SPLB31A State Diagram*”	6
		2. Correct “SPRS512A” to “SRS512C”, “SPRS1024A” to “SPRS1024C”	5
		3. Modify LCD driver voltage Max. value from “5.70V” to “5.75V”	6, 9
		4. Update PIN No. in the “*5. SIGNAL DESCRIPTIONS*”	4
		5. Add 7.3, 7.4, 7.5 sections in the “*7. ELECTRICAL SPECIFICATIONS*”	10
		6. Correct chip size	15
		7. Add Note1 in the “*9.1 PAD Assignment*”	15
		8. Add “Note: Pin VROUT should be connected to VDD if internal Regulator is disabled.” in the “*5. SIGNAL DESCRIPTIONS*” 、“*8. APPLICATION CIRCUIT*” and “*9.1 PAD Assignment*”	
		9. Renew to a new document format	