RMPA0913C-58
3.5V AMPS/CDMA Power Amplifier

Description

The RMPA0913C-58 is a monolithic high efficiency power amplifier for AMPS/ CDMA dual mode applications in the 824 to 849 MHz frequency band. Performance parameters may be slightly adjusted by "tweaking" off-chip matching components. The amplifier circuit design is a single ended configuration that utilizes harmonic tuning for increased power added efficiency and linearity. The device uses Raytheon's Pseudomorphic High Electron Mobility Transistor (pHEMT) process.

Features

- Positive supply voltage of 3.5V, nominal
- Power Added Efficiency of 56%, typical, at power out of 31.5 dBm
- Power Added Efficiency of 40%, typical, for CDMA power out of 28.5 dBm
- Small outline metal based quad plastic package

Electrical Characteristics

(Specifications at 25 ^{o}C operating free air temperature unless otherwise stated)

Parameter	Min	Typ	Max	Unit
Frequency Range	824		849	MHz
Gain (Small Signal)		30.0		dB
Gain Variation vs Temp		-0.02		dB/°C
Gain Linearity				
(0 dBm ≤ Pout ≤ 28.5 dBm)	-1.5		+0.0	dB
Noise Power (869-894 MHz)			-140	dBm/Hz
Input VSWR (50Ω)			2.0:1	---
Stability (All spurious) [1]			-70	dBc
Harmonics (Po ≤ 31.5 dBm)			-35	dBc
Power Out				
Vdd=3.5V, Pin=7 dBm		32.5		dBm
Efficiency				
Pin = 7 dBm, Vdd=3.5V		62		%
Po = 31.5 dBm, Vdd = 3.5V		56		%
Po = 28.5 dBm, Vdd=3.5V		40		%
Po = 10 dBm, Vdd=3.5V		1.5		%
ACPR [2] (Offset ≥ ± 900 kHz)		48		dBc
(Offset ≥ ± 1.98 MHz)		63		dBc
Noise Figure (over temp)			4.5	dB
Vdd		3.5		Volts
Vg1, Vg2 (<4 mA)[3]	-1.75		-0.25	Volts
Case Operating Temp	-40		+85	°C

Notes:
1. Source/Load VSWR (All Angles) ≤ 3:1 In-Band, Load VSWR (All Angles) ≥ 20:1 Out of Band, Valid over Case Operating Temperature Range.
2. Po ≤ 28.5 dBm at Vdd=3.5V; CDMA Waveform measured using the ratio of the average power within a 1.23 MHz channel and within a 30 kHz bandwidth at the specified offset.
3. Vg1 adjusted for Idq (stage 1) = 35 mA, Vg2 adjusted for Idq (stage 2) = 155 mA.

Product Information

Tel: 978-684-8663
FAX: 978-684-5480
www.raytheon.com/micro

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Raytheon RF Components
362 Lowell Street
Andover, MA 01810

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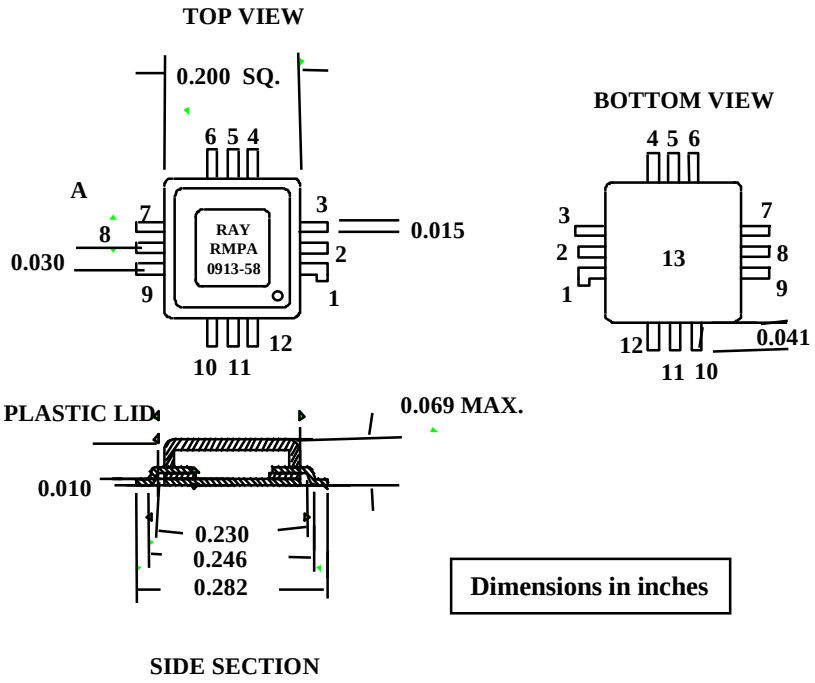
Product Information

Package Data



Pin#	Description
1	RF Out & Vd2
2	RF Out & Vd2
3	RF Out & Vd2
4	AC Ground (g2)
5	GND
6	AC Ground (g1)
7	GND
8	RF Input
9	GND
10	Vd1
11	Vg2
12	Vg1
13	GND (METAL BASE)

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Application Information for the RMPA0913C-58

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following describes a procedure for evaluating the Raytheon RMPA0913C-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use in the AMPS/CDMA dual mode portable phones. Figure 1 shows the package outline and pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that the amplifier requires external passive components for DC bias and RF input and output matching circuits. A recommended schematic is shown in figure 3. The gate biases for the two stages of the amplifier are set by simple on-chip circuits. Figure 4 shows a typical layout of an evaluation board (RMPA0913C-58-TB), corresponding to the schematic circuit of figure 3. The following should be noted:

(1) Pin designations and their functions are as shown in figure 1 and Table 1.
(2) Vg1, Vg2 are denoted as the Gate Voltages (negative) applied at the pins of the package
(3) Vgg1, Vgg2 are denoted as the negative supply voltages at the evaluation board terminals
(4) Vd1, Vd2 are denoted as the Drain Voltages (positive) applied at the pins of the package
(5) Vdd1, Vdd2 are denoted as the positive supply voltages at the evaluation board terminals

Note: the two drain voltages are tied to the same terminal denoted as Vdd on the evaluation board

Test Procedure for the evaluation board (RMPA0913C-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE DRAIN VOLTAGES (VD1,VD2) ARE PRESENT MAY DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Slowly apply gate supply voltages of -3.0 V to the board terminals Vgg1, Vgg2 to pinch-off the two stages.

Step 3: Slowly apply drain supply voltage of +3.5 V to the board terminals Vdd.

Step 4: Adjust the gate supply voltages Vgg1, Vgg2 to the values shown on the data summary supplied with the sample. (First adjust Vgg2 to set Idq2. Then adjust Vgg1 to set Iddq=Idq1+Idq2. These gate voltages need not be changed. However, Vgg1,Vgg2 may be adjusted only when different quiescent bias currents are desired for performance trade-off evaluation).

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band. Adjust RF input signal power level as required.

Step 6: Follow turn-off sequence of:
(i) Turn off RF Input Power (ii) Turn down and off drain voltage Vdd.
(iii) Turn down and off gate voltages Vgg1, Vgg2.

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Maximum Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage	Vd1,Vd2	+ 9	Volts
Negative DC Voltage	Vg1,Vg2	- 6	Volts
Simultaneous (Vd-Vg)	Vdg	+12	Volts
RF Input Power (from 50-Ohm source)	P_{IN}	+10	dBm
Operating Case Temperature (Case)	T_C	-30 to 110	°C
Storage Temperature Range	T_{Stg}	-35 to 110	°C
Thermal Resistance	RTj-c	15	°C/W

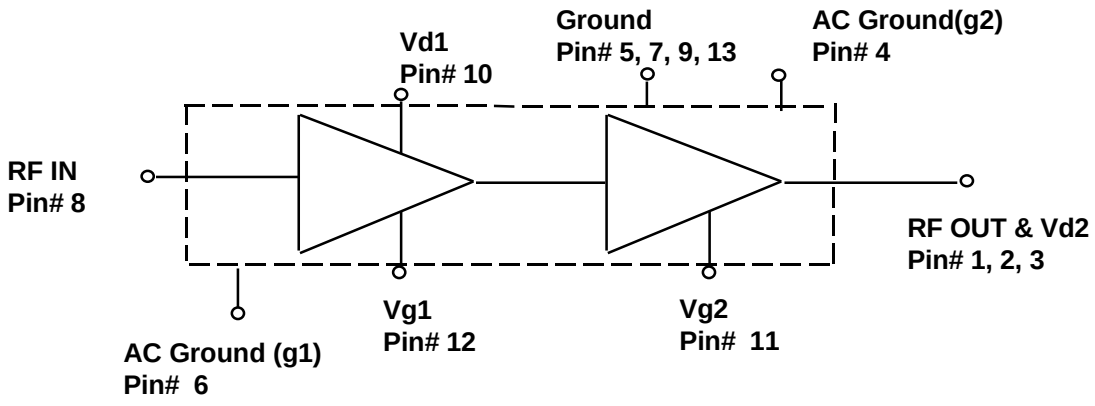

Figure 1: Functional Block Diagram of Packaged Product (RMPA0913C-58)

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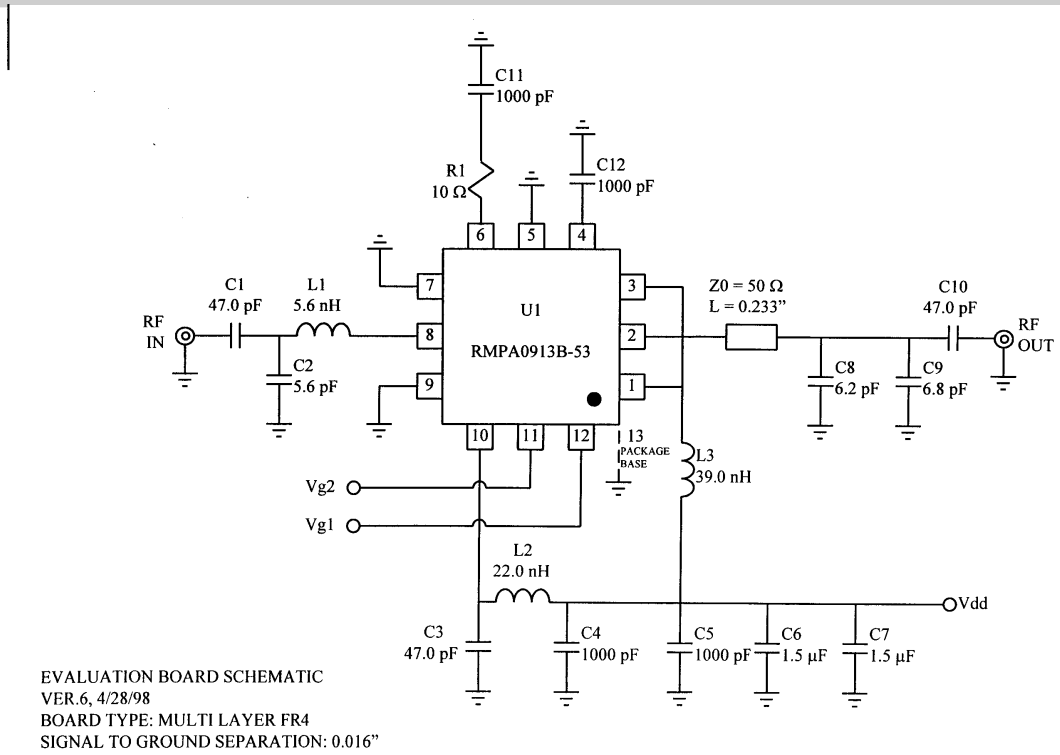

Figure 3: Schematic for a Typical Test Evaluation Board

PARTS LIST for Test Evaluation Board (RMPA0913C-58-TB)

PART	VALUE	EIA SIZE	Vendor(s)
C1,C3,C10	47 pF	0402	Murata, GRM36COG470J050
C2	5.6 pF	0402	Murata, GRM36COG5R6B050
C8	6.2 pF	0402	Murata, GRM36COG6R2B050
C9	6.8 pF	0402	Murata, GRM36COG6R8B050
C4,C5,C11,C12	1000 pF	0402	Murata, GRM36X7R102K050
C6,C7	1.5 uF	3528	Kemet (T494B155K020AS)
L1	5.6 nH	0603	Toko, LL1608-FH5N6S
L2	22 nH	0603	Toko, LL608-FH22NK
L3	39 nH	1008	Coilcraft, 1008HS-390TKBC
R1	10 Ohm	0402	IMS, RCI-0402-10R0J
W1	26AWG (0.015" dia) Wire		Alpha, 2853/1
U1	RMPA0913C-58, 3.5V PA		Raytheon, G655923
P3	Right angle Pin Header		3M (2340-5211TN)
P1,P2	SMA Connectors		Johnson Components (142-0701-841)
Board	FR4		Raytheon Dwg# G654626, V1

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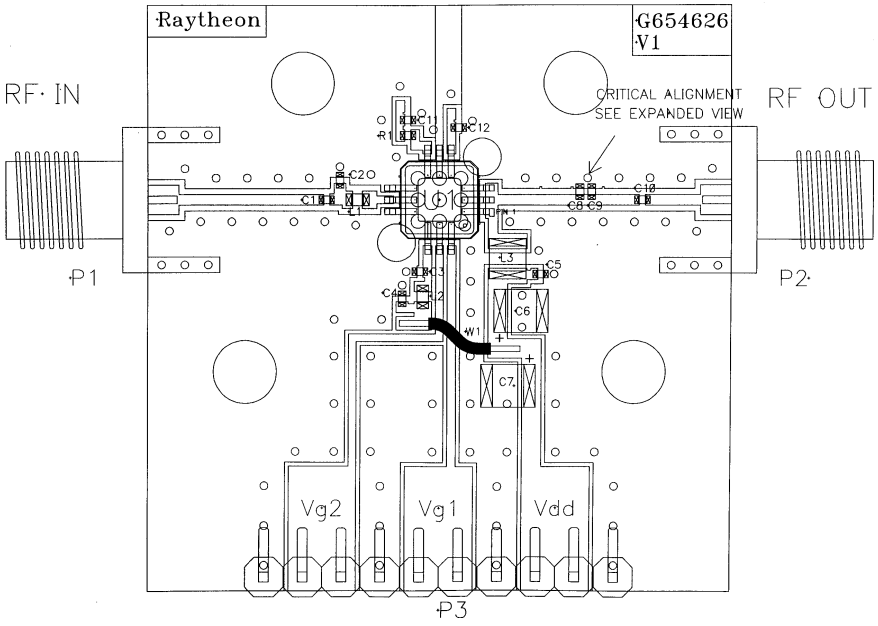

Figure 4: Layout and Assembly of Test Evaluation Board

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Table 1: Further Important Application Information

Pin#	Function	Application Notes
1	RF OUT AND VD2	An optimal output match for dual mode applications is set by connecting capacitors C8 and C9 to the package pin using approximately 0.233 inches of a 50 ohm transmission line. These capacitors should be located adjacent to each other and separated by 0.010 inches. Lower efficiency will result if a single capacitor of equivalent value were substituted. Fine adjust the capacitors location to obtain a uniform saturated output power response versus frequency using a single tone RF input. Saturated output power is typically measured at +7dBm input power and should be 32.3 to 32.5dBm with a 3.5 volt supply. This condition will yield typically 50dBc ACPR1 and 60dBc ACPR2 at 28.5dBm output power at 3.5 volt supply using a CDMA waveform. If a greater than 50 ohm impedance transmission line is used to conserve space, transition the line to 50 ohms slightly prior to the optimum tuning point to avoid undesirable effects from the otherwise residual inductance following the tuning elements. Once the optimum tuning point has been established this remains fixed for all other amplifiers. For the dc bias injection circuit choose an inductor with a maximum series resistance rating of less than 0.15 ohms for best efficiency and overall performance versus supply voltage. The two 1.5uF tantalum bypass capacitors chosen for this circuit are low ESR type capacitors with a maximum rating of 1.5 ohms. The capacitor ESR is critical for achieving the best ACPR possible from the amplifier. Other capacitors may be substituted, although larger values may be necessary to achieve equivalent performance. These components should be placed at the tie point for VD1 and VD2 and as close to the amplifier as possible. Finally, connect pins 1-3 using one solid metal pad as opposed to three individual pads for each pin.
2	RF OUT AND VD2	Same as pin 1.
3	RF OUT AND VD2	Same as pin 1.
4	G2 AC GND	Place component C12 $\leq$ 0.080 inches from the package pin.
5	GND	Connect pin immediately to the package base solder pad.

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Table 1: Further Important Application Information (cont'd)

Pin#	Function	Application hints
6	G1 AC GND	Place components R1 and C11 ≤ 0.080 inches from the package pin.
7	GND	Same as pin 5.
8	RF IN	The amplifier input is optimally matched to 50 ohms by locating capacitor C2 at a distance of 0.138 inches from the package pin. If it is not possible to obtain this separation, adjust the value of inductor L1 to compensate and obtain the desired match.
9	GND	Same as pin 5.
10	VD1	Place component C3 ≤ 0.080 inches from the package pin. The dc resistance of inductor L2 should be <= 0.5 ohms to obtain optimum amplifier performance. Also, connect VD1 and VD2 at the board component surface and route VG1 and VG2 bias lines to other conductor layers to minimize any additional ohmic losses on the drain supply line.
11	VG2	Connect to a low impedance negative voltage power supply for stage 2 current control. From pinchoff, adjust VG2 voltage to achieve 155mA of stage 2 current, ID2. This current is optimum for high power CDMA operation up to 28.5dBm output power. For improved performance, adjust to lower current for low power CDMA and analog modes of operation. Since both stage 1 and stage 2 drains contribute to the total amplifier current the first stage must be pinched off while adjusting VG2 for a specific ID2 current. A pinchoff condition is achieved by applying -2.0 to -5.0 volts to the gate pins, VG1 and VG2.
12	VG1	Connect to a low impedance negative voltage power supply for stage 1 current control, ID1. From pinchoff, adjust VG1 voltage to achieve 35mA of stage 1 current.
13	PACKAGE BASE AND GND	The solder pad for this package should be 0.210 inches square. Fill the pad with several plated-thru vias connecting the pad surface to the RF input and output ground planes. Insufficient grounding of the package base may cause the amplifier to oscillate or result in poor amplifier performance.